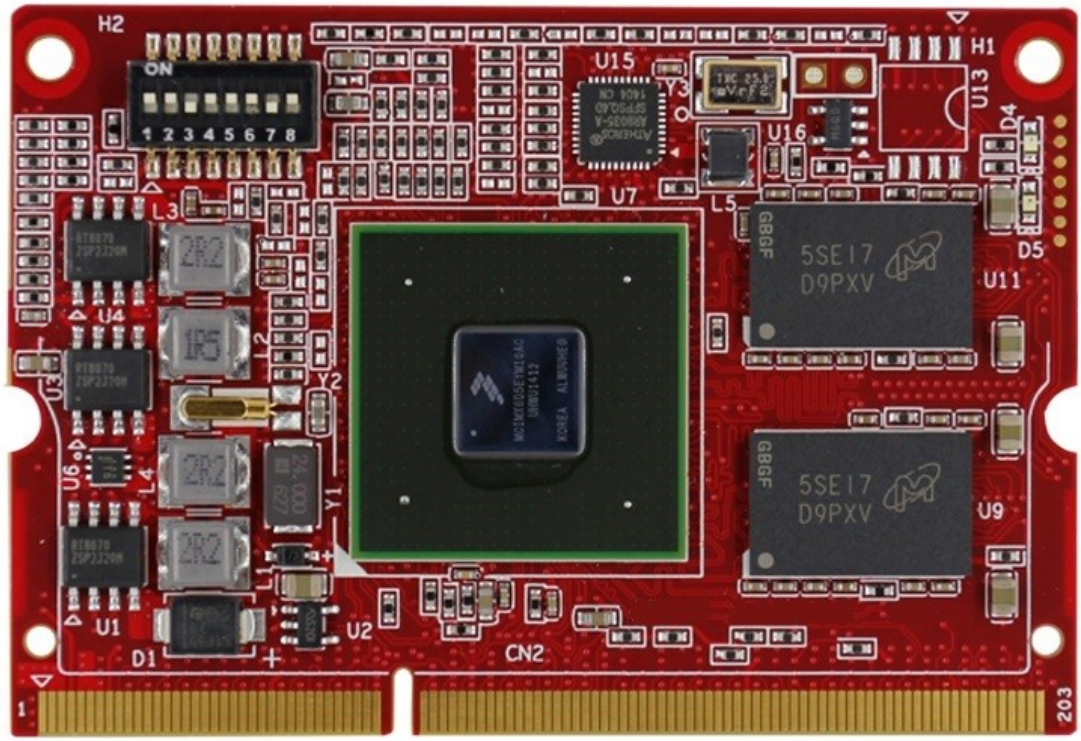
VERA Imx6 Module Hardware Manual
Rev 1.0



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Revision History..

Rev.	Document Code	Released	Written	Verified	Approved
1.0	**VERA Imx6 Module Hardware Manual**	Data	Autore	Data	Approvatore

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1 Chapter 1 Product Overview

1.1 Introduction

1.2 Hardware

The VERA is a core module based on the NXP(Freescale) IMX6 Cortex-A9 processor. The core module is Measured only 67.6mm X 46mm, integrates 1G/2GBytes DDR3 SDRAM and up to 8GBytes eMMC flash. It offers a wide range of interfaces from simple GPIOs, industry standard I2C, SPI, CAN, CSI, LVDS, SATA, PCIE and UART buses through to high speed USB 2.0 interface, and gigabit Ethernet.

The module targets a wide range of applications, including: HMIs, Digital Signage, POS, Data Terminal, Medical Devices, Navigation, Industrial Automation, Entertainment system, Thin Clients, Robotics, Game Console and much more.

1.3 Software

The VERA is a ready-to-run platform to support for Linux 4.x, Android 6.x operating systems.

If you care about other Operating System, For more information contact our support.

1.4 Product Overview

The following sections list out all the porduct features.

Series	Vera Dual	Vera Dual	Vera Quad	Vera Quad
Part Code	VRAD0011	VRAD0021	VRAQ0021	VRAQ0011
CPU Name	NXP(Freescale) IMX6 dual core	NXP(Freescale) IMX6 dual core	NXP(Freescale) IMX6 quad core	NXP(Freescale) IMX6 quad core
CPU Type	ARM Cortex™-A9	ARM Cortex™-A9	ARM Cortex™-A9	ARM Cortex™-A9
CPU Clock	2x	2x	4x	4x
CPU Frequency	1GHz	1GHz	1GHz	1GHz
RAM DDR3	Micron 1GB@16bit*4	Micron 2GB@16bit*4	Micron 2GB@16bit*4	Micron 1GB@16bit*4
Flash	eMMC 4GB@8bit*1	eMMC 4GB@8bit*1	eMMC 4GB@8bit*1	eMMC 4GB@8bit*1
Size	67.6 x 46 x 6.2mm	67.6 x 46 x 6.2mm	67.6 x 46 x 6.2mm	67.6 x 46 x 6.2mm
Temperature	0° to 70° C	0° to 70° C	0° to 70° C	0° to 70° C
Support OS	Linux 4.x Android 6.x	Linux 4.x Android 6.x	Linux 4.x Android 6.x	Linux 4.x Android 6.x

2 Chapter 2 Hardware System

Block Diagram

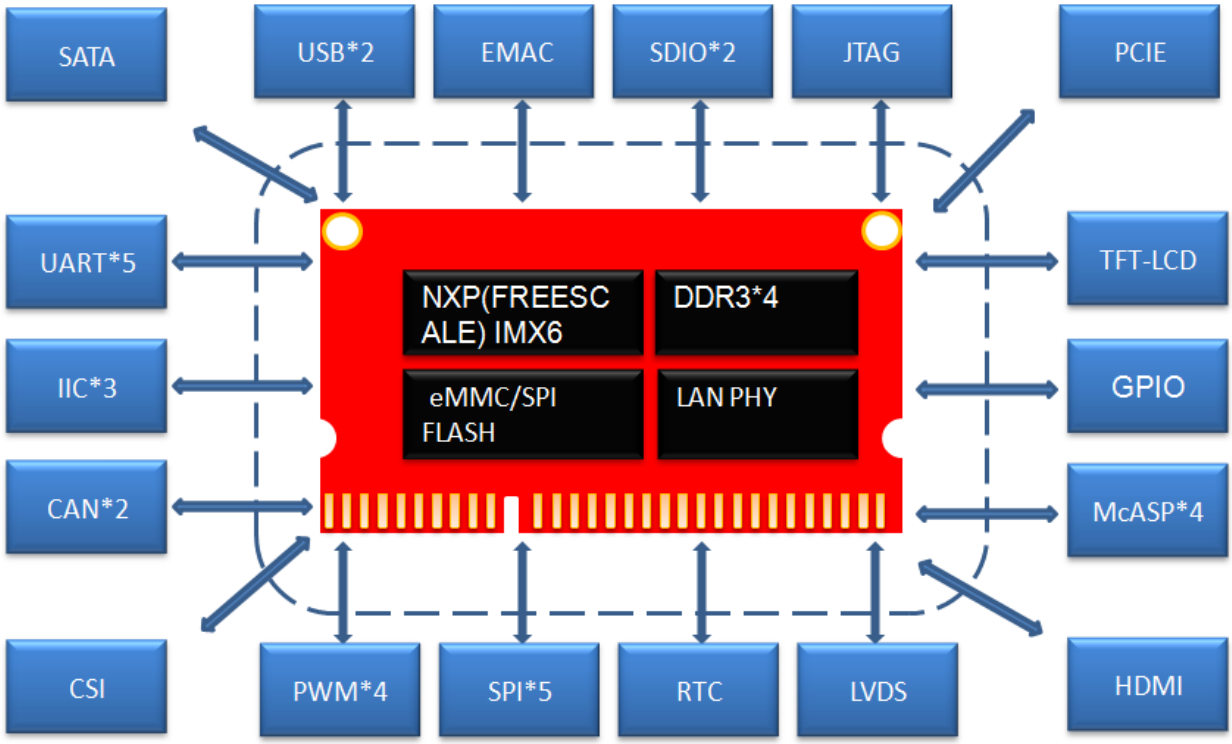


Figure 1 VERA Block Diagram

2.1 Main Features

2.1.1 CPU

Series	Vera Dual	Vera Dual	Vera Quad	Vera Quad
Part Code	VRAD0011	VRAD0021	VRAQ0021	VRAQ0011
CPU Name	NXP(Freescale) IMX6 dual core	NXP(Freescale) IMX6 dual core	NXP(Freescale) IMX6 quad core	NXP(Freescale) IMX6 quad core
ARM CPU	ARM Cortex™-A9	ARM Cortex™-A9	ARM Cortex™-A9	ARM Cortex™-A9
CPU Frequency	1GHz	1GHz	1GHz	1GHz
NEON MPE coprocessor	1	1	1	1
Graphics Acceleration	1 3D	1 3D	1 3D	1 3D
Other Hardware Accelertaion	● VPU-Video ● Two IPUv3H-Image ● GPU2Dv2-2D graphics ● GPU VG-Open VG1.1 graphics ● ASRC-Asynchronous sample rate converter	● VPU-Video ● Two IPUv3H-Image ● GPU2Dv2-2D graphics ● GPU VG-Open VG1.1 graphics ASRC-Asynchronous sample rate converter	● VPU-Video ● Two IPUv3H-Image ● GPU2Dv2-2D graphics ● GPU VG-Open VG1.1 graphics ASRC-Asynchronous sample rate converter	● VPU-Video ● Two IPUv3H-Image ● GPU2Dv2-2D graphics ● GPU VG-Open VG1.1 graphics ASRC-Asynchronous sample rate converter
On-Chip L1 Cache	64KB	64KB	64KB	64KB
On-Chip L2 Cache	1MB	1MB	1MB	1MB
Other On-Chip Memory	L1 cache: 64KB L2 cache: 1MB	L1 cache: 64KB L2 cache: 1MB	L1 cache: 64KB L2 cache: 1MB	L1 cache: 64KB L2 cache: 1MB
Display Options	LCD	LCD	LCD	LCD
General Purpose Memory	1 16-bit (GPMC, NAND flash, NOR flash, SRAM)	1 16-bit (GPMC, NAND flash, NOR flash, SRAM)	1 16-bit (GPMC, NAND flash, NOR flash, SRAM)	1 16-bit (GPMC, NAND flash, NOR flash, SRAM)
DRAM	4 16-bit (LPDDR2-1066,LV-DDR3-1066,DDR3-1066)	4 16-bit (LPDDR2-1066,LV-DDR3-1066,DDR3-1066)	4 16-bit (LPDDR2-1066,LV-DDR3-1066,DDR3-1066)	4 16-bit (LPDDR2-1066,LV-DDR3-1066,DDR3-1066)
USB	2	2	2	2

Series	Vera Dual	Vera Dual	Vera Quad	Vera Quad
EMAC	10/100/1000	10/100/1000	10/100/1000	10/100/1000
SDIO	3	3	3	3
CAN	2	2	2	2
UART (SCI)	5	5	5	5
SATA	SATA II 3.0Gbps	SATA II 3.0Gbps	SATA II 3.0Gbps	SATA II 3.0Gbps
SPI Flash	16Mbit	16Mbit	16Mbit	16Mbit
PCI Express	Gen 2.0 one lane	Gen 2.0 one lane	Gen 2.0 one lane	Gen 2.0 one lane
PWM	4	4	4	4
HDMI	1	1	1	1
RGB	24bit	24bit	24bit	24bit
LVDS	1	1	1	1
CSI Parrallel	1	1	1	1
MIPI CSI	1	1	1	1
RTC	1	1	1	1
IIC	3	3	3	3
McASP	4	4	4	4
SPI	5	5	5	5

Series	Vera Dual	Vera Dual	Vera Quad	Vera Quad
IO Supply (V)				
	3.3	3.3	3.3	3.3

2.1.2 Memory

Series	Monkey™	Monkey™	Monkey™	Monkey™
Part Code	CM6D5E X1	CM6D5E X2	CM6Q5E X1	CM6Q5E X2
DDR3 RAM Size	2GByte	1GByte	2GByte	1GByte
DDR3 RAM Speed	800MT/S	800MT/S	800MT/S	800MT/S
DDR3 RAM Memory Width	16bit	16bit	16bit	16bit
eMMC (8bit)	8GByte	4/8GByte	8GByte	4/8GByte

2.1.3 Interface

Series	Vera Dual	Vera Dual	Vera Quad	Vera Quad
Part Code	VRAD0011	VRAD0021	VRAQ0021	VRAQ0011
USB	2	2	2	2
SDIO	2	2	2	2
UART	3+2*	3+2*	3+2*	3+2*
SPI	2+3*	2+3*	2+3*	2+3*
IIC	3	3	3	3
EMAC	1	1	1	1
PWM	0+4*	0+4*	0+4*	0+4*
CAN	1+1*	1+1*	1+1*	1+1*
HDMI	1	1	1	1
RGB	1	1	1	1
LVDS	1	1	1	1
CSI	2	2	2	2
PCIE	1	1	1	1
SATA	1	1	1	1
GPIO	12+112*	12+112*	12+112*	12+112*
JTAG	1	1	1	1
RTC	1	1	1	1
McASP	1+3*	1+3*	1+3*	1+3*

🕮 *These interfaces are available on pins that are not defined as standard interfaces in the core module. Some of the pins are multiplexed for other functions. Please refer to the CPU datasheet and schematics for details.

2.2 Reference Documents

2.2.1 CPU IMX6

IMX6 is a CPU used on VERA.
If you need more information about the CPU, please refer to http://www.nxp.com

2.2.2 Ethernet PHY AR8035-AL1B-R

AR8035-AL1B-R is a PHY of Giga LAN used on CM335N.
If you need more information about the PHY, please refer to AR8035-AL1B-R from http://www.atheros.com

2.2.3 DDR3 MT41K256M16HA-125:E

MT41K256M16HA-125:E is a 512M DDR3 Memory used on VERA.
If you need more information about the DDR3, please refer to MT41K256M16HA-125:E from http://www.micron.com

2.2.4 eMMC flash MTFC4GMVEA-0M WT/MTFC8GLVEA-4MIT

MTFC4GMVEA-0M WT/MTFC8GLVEA-4MIT is a 4GB/8GB eMMC flash used on VERA.
If you need more information about the eMMC, please refer to MTFC4GMVEA-0M WT/MTFC8GLVEA-4MIT from http://www.micron.com

2.4 Hardware Interfaces

2.4.1 CN1 Interface

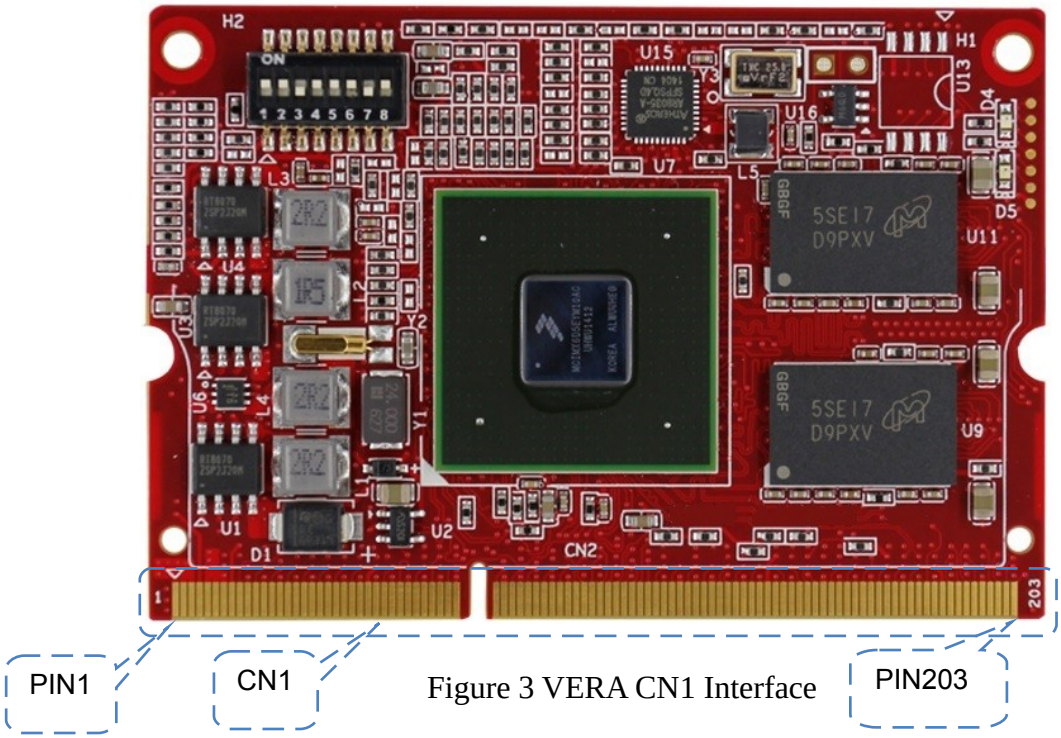


Figure 3 VERA CN1 Interface

Pin	Signal name	Description	I/O	Power rail	Note
1	5VIN	5V main power supply	P	5V	
2	GND	Digital ground		GND	
3	5VIN	5V main power supply	P	5V	
4	GND	Digital ground		GND	
5	5VIN	5V main power supply	P	5V	
6	GND	Digital ground		GND	
7	5V_CONTRRL	5V main power supply control	I	5V	
8	NC	Not connected			
9	3P3V	3.3V main power supply	P	3.3V	
10	2P5V	2.5V main power supply	P	2.5V	
11	3P3V	3.3V main power supply	P	3.3V	
12	RGMII_VDD2V5	2.5V lan power supply	P	2.5V	
13	3P3V	3.3V main power supply	P	3.3V	
14	OTG_VBUS	5V USB OTG power supply	P	5V	

Pin	Signal name	Description	I/O	Power rail	Note
15	VDD_RTC	RTC backup power supply	P	3V	
16	NC	Not connected			
17	POR_B	System reset	I	3.3V	
18	DISP0_DAT0	LCD data bus	I/O	3.3V	
19	GPIO1_27	GPIO	I/O	3.3V	
20	DISP0_DAT1	LCD data bus	I/O	3.3V	
21	LCD_PWR_EN	LCD power enable	O	3.3V	
22	DISP0_DAT2	LCD data bus	I/O	3.3V	
23	UART2_TXD	UART transmit data	O	3.3V	
24	DISP0_DAT3	LCD data bus	I/O	3.3V	
25	UART2_RXD	UART receive data	I	3.3V	
26	DISP0_DAT4	LCD data bus	I/O	3.3V	
27	UART2_CTS	UART clear to send	O	3.3V	
28	DISP0_DAT5	LCD data bus	I/O	3.3V	
29	UART2_RTS	UART request to send	I	3.3V	
30	DISP0_DAT6	LCD data bus	I/O	3.3V	
31	CSPI1_CLK	SPI clock	I/O	3.3V	
32	DISP0_DAT7	LCD data bus	I/O	3.3V	
33	CSPI1_MISO	SPI master input, slave output	I	3.3V	
34	DISP0_DAT8	LCD data bus	I/O	3.3V	
35	CSPI1_MOSI	SPI master output, slave input	O	3.3V	
36	DISP0_DAT9	LCD data bus	I/O	3.3V	
37	CSPI1_CS1	SPI chip select	I/O	3.3V	
38	DISP0_DAT10	LCD data bus	I/O	3.3V	
39	CSPI4_CLK	SPI clock	I/O	3.3V	
40	DISP0_DAT11	LCD data bus	I/O	3.3V	
41	CSPI4_MISO	SPI master input, slave output	I	3.3V	
42	DISP0_DAT12	LCD data bus	I/O	3.3V	
43	CSPI4_MOSI	SPI master output, slave input	O	3.3V	
44	DISP0_DAT13	LCD data bus	I/O	3.3V	
45	CSPI4_CS0	SPI chip select	I/O	3.3V	
46	DISP0_DAT14	LCD data bus	I/O	3.3V	
47	CSPI4_CS1	SPI chip select	I/O	3.3V	
48	DISP0_DAT15	LCD data bus	I/O	3.3V	
49	GND	Digital ground		GND	
50	DISP0_DAT16	LCD data bus	I/O	3.3V	
51	SD2_CLK	MMC/SD/SDIO clock	I/O	3.3V	
52	DISP0_DAT17	LCD data bus	I/O	3.3V	
53	SD2_DATA0	MMC/SD/SDIO data bus	I/O	3.3V	
54	DISP0_DAT18	LCD data bus	I/O	3.3V	
55	SD2_DATA1	MMC/SD/SDIO data bus	I/O	3.3V	
56	DISP0_DAT19	LCD data bus	I/O	3.3V	

Pin	Signal name	Description	I/O	Power rail	Note
57	SD2_DATA2	MMC/SD/SDIO data bus	I/O	3.3V	
58	DISP0_DAT20	LCD data bus	I/O	3.3V	
59	SD2_DATA3	MMC/SD/SDIO data bus	I/O	3.3V	
60	DISP0_DAT21	LCD data bus	I/O	3.3V	
61	SD2_DATA4	MMC/SD/SDIO data bus	I/O	3.3V	
62	DISP0_DAT22	LCD data bus	I/O	3.3V	
63	SD2_DATA5	MMC/SD/SDIO data bus	I/O	3.3V	
64	DISP0_DAT23	LCD data bus	I/O	3.3V	
65	SD2_DATA6	MMC/SD/SDIO data bus	I/O	3.3V	
66	DISP0_HSYNC	LCD horizontal sync	O	3.3V	
67	SD2_DATA7	MMC/SD/SDIO data bus	I/O	3.3V	
68	DISP0_VSYNC	LCD vertical sync	O	3.3V	
69	SD2_WP	MMC/SD/SDIO data write protect	O	3.3V	
70	DISP0_DRDY	LCD enable	O	3.3V	
71	SD2_CMD	MMC/SD/SDIO command	I/O	3.3V	
72	DISP0_CLK	LCD pixel clock	O	3.3V	
73	SD2_CD	SD card detect	I	3.3V	
74	UART3_CTS	UART clear to send	O	3.3V	
75	GND	Digital ground		GND	
76	UART3_RTS	UART request to send	I	3.3V	
77	SD1_CLK	MMC/SD/SDIO clock	I/O	3.3V	
78	UART3_TXD	UART transmit data	O	3.3V	
79	SD1_WP	MMC/SD/SDIO data write protect	O	3.3V	
80	UART2_RXD	UART receive data	I	3.3V	
81	SD1_CMD	MMC/SD/SDIO command	I/O	3.3V	
82	GND	Digital ground		GND	
83	SD1_CD	SD card detect	I	3.3V	
84	SATA_RXP	Positive differential SATA receive signal	I		
85	SD1_DATA0	MMC/SD/SDIO data bus	I/O	3.3V	
86	SATA_RXN	Negative differential SATA receive signal	I		
87	SD1_DATA1	MMC/SD/SDIO data bus	I/O	3.3V	
88	SATA_TXN	Negative differential SATA transmit signal	O		
89	SD1_DATA2	MMC/SD/SDIO data bus	I/O	3.3V	
90	SATA_TXP	Positive differential SATA transmit signal	O		
91	SD1_DATA3	MMC/SD/SDIO data bus	I/O	3.3V	
92	GND	Digital ground		GND	
93	SD1_DATA4	MMC/SD/SDIO data bus	I/O	3.3V	
94	PCIE_RXM	Negative differential PCIE receive signal	I		
95	SD1_DATA5	MMC/SD/SDIO data bus	I/O	3.3V	
96	PCIE_RXP	Positive differential PCIE receive signal	I		
97	SD1_DATA6	MMC/SD/SDIO data bus	I/O	3.3V	
98	PCIE_TXM	Negative differential PCIE transmit signal	O		

Pin	Signal name	Description	I/O	Power rail	Note
99	SD1_DATA7	MMC/SD/SDIO data bus	I/O	3.3V	
100	PCIE_TXP	Positive differential PCIE transmit signal	O		
101	GPIO7_6	GPIO	I/O	3.3V	
102	PCIE_WAKEn	Wake-up by PCIE	I	3.3V	
103	UART1_RXD	UART receive data	I	3.3V	
104	PRSNT2_N_X1	PCIE reset	O	3.3V	
105	UART1_TXD	UART transmit data	O	3.3V	
106	PCIE_REFCLK_DN	Negative differential PCIE reference clock signal	O		
107	uP_NMin	Touch panel interrupt	O	3.3V	
108	PCIE_REFCLK_DP	Positive differential PCIE reference clock signal	O		
109	GPIO6_9	GPIO	I/O	3.3V	
110	GND	Digital ground		GND	
111	GPIO6_16	GPIO	I/O	3.3V	
112	HDMI_D2P	Positive differential HDMI transmit signal of channel 2	O		
113	GPIO6_7	GPIO	I/O	3.3V	
114	HDMI_D2M	Negative differential HDMI transmit signal of channel 2	O		
115	GPIO6_10	GPIO	I/O	3.3V	
116	HDMI_D1P	Positive differential HDMI transmit signal of channel 1	O		
117	GPIO6_15	GPIO	I/O	3.3V	
118	HDMI_D1M	Negative differential HDMI transmit signal of channel 1	O		
119	GND	Digital ground		GND	
120	HDMI_D0P	Positive differential HDMI transmit signal of channel 0	O		
121	USB_HOST_DN	Negative differential USB signal	I/O	5V	
122	HDMI_D0M	Negative differential HDMI transmit signal of channel 0	O		
123	USB_HOST_DP	Positive differential USB signal	I/O	5V	
124	HDMI_CLKP	Positive differential HDMI clock signal	O		
125	USB_RSTn	USB reset	O		
126	HDMI_CLKM	Negative differential HDMI clock signal	O		
127	GND	Digital ground		GND	
128	HDMI_HPD	HDMI hot plug detection	I		
129	USB_OTG_DN	Negative differential USB OTG signal	I/O	5V	
130	GND	Digital ground		GND	
131	USB_OTG_DP	Positive differential USB signal	I/O	5V	
132	I2C1_SDA	I2C data	I/O	3.3V	
133	USB_OTG_ID	Use this pin to detect the ID pin if you use USB OTG.	I	5V	
134	I2C1_SCL	I2C clock	I/O	3.3V	

Pin	Signal name	Description	I/O	Power rail	Note
135	USB_H1_OC	USB host over current signal	I	3.3V	
136	CAN1_TXD	DCAN transmit data	O	3.3V	
137	USB_OTG_PWR_EN	USB OTG power enable	O	3.3V	
138	CAN1_RXD	DCAN receive data	I	3.3V	
139	USB_OTG_OC	USB OTG over current signal	I	3.3V	
140	I2C3_SCL	I2C clock	I/O	3.3V	
141	GND	Digital ground		GND	
142	I2C3_SDA	I2C data	I/O	3.3V	
143	CSI_CLK0M	Negative differential CSI clock signal			
144	UART5_TXD	UART transmit data	O	3.3V	
145	CSI_CLK0P	Positive differential CSI clock signal			
146	UART5_RXD	UART receive data	I	3.3V	
147	CSI_D0M	Negative differential CSI signal of channel 0	I		
148	I2C2_SCL	I2C clock	I/O	3.3V	
149	CSI_D0P	Positive differential CSI signal of channel 0			
150	I2C2_SDA	I2C data	I/O	3.3V	
151	CSI_D1M	Negative differential CSI signal of channel 1			
152	GPIO7_1	GPIO	I/O	3.3V	
153	CSI_D1P	Positive differential CSI signal of channel 1			
154	GPIO1_1	GPIO	I/O	3.3V	
155	GND	Digital ground		GND	
156	Touch_Int	Touch panel interrupt	O	3.3V	
157	CSI0_DAT12	CSI data bus	I/O	3.3V	
158	LED_PWR_EN	LED power enable	O	3.3V	
159	CSI0_DAT13	CSI data bus	I/O	3.3V	
160	RESET_N_B	Reset signal	O	3.3V	
161	CSI0_DAT14	CSI data bus	I/O	3.3V	
162	GND	Digital ground		GND	
163	CSI0_DAT15	CSI data bus	I/O	3.3V	
164	LVDS0_TX3_N	Negative differential LVDS transmit signal of channel 3			
165	CSI0_DAT16	CSI data bus	I/O	3.3V	
166	LVDS0_TX3_P	Positive differential LVDS transmit signal of channel 3			
167	CSI0_DAT17	CSI data bus	I/O	3.3V	
168	LVDS0_TX2_N	Negative differential LVDS transmit signal of channel 2			
169	CSI0_DAT18	CSI data bus	I/O	3.3V	
170	LVDS0_TX2_P	Positive differential LVDS transmit signal of channel 2			
171	CSI0_DAT19	CSI data bus	I/O	3.3V	
172	LVDS0_TX1_N	Negative differential LVDS transmit signal of channel 1			
173	CSI0_PIXCLK	CSI pixel clock	O	3.3V	

Pin	Signal name	Description	I/O	Power rail	Note
174	LVDS0_TX1_P	Positive differential LVDS transmit signal of channel 1			
175	CSI0_HSYNC	CSI horizontal sync	O	3.3V	
176	LVDS0_TX0_N	Negative differential LVDS transmit signal of channel 0			
177	CSI0_VSYNC	CSI vertical sync	O	3.3V	
178	LVDS0_TX0_P	Positive differential LVDS transmit signal of channel 0			
179	CAM_RST	CSI reset	O	3.3V	
180	LVDS0_CLK_P	Positive differential LVDS clock signal			
181	CAM_EN	CSI enable	O	3.3V	
182	LVDS0_CLK_N	Negative differential LVDS clock signal			
183	CAM_MCLK	CSI master clock	O	3.3V	
184	GND	Digital ground		GND	
185	GND	Digital ground		GND	
186	TRP0	Positive differential media-dependent interface 0 of Giga LAN			
187	AUD3_TXC	I2S bit clock	O	3.3V	
188	TRN0	Negative differential media-dependent interface 0 of Giga LAN			
189	AUD3_TXD	I2S transmit data	O	3.3V	
190	TRP1	Positive differential media-dependent interface 1 of Giga LAN			
191	AUD3_TXFS	I2S frame clock	O	3.3V	
192	TRN1	Negative differential media-dependent interface 1 of Giga LAN			
193	AUD3_RXD	I2S receive data	I	3.3V	
194	TRP2	Positive differential media-dependent interface 2 of Giga LAN			
195	GND	Digital ground		GND	
196	TRN2	Negative differential media-dependent interface 2 of Giga LAN			
197	GPIO1_9	GPIO	I/O	3.3V	
198	TRP3	Positive differential media-dependent interface 3 of Giga LAN			
199	TP_BUSY	Touch panel busy signal	I	3.3V	
200	TRN3	Negative differential media-dependent interface 3 of Giga LAN			
201	GPIO4_7	GPIO	I/O	3.3V	
202	LED_ACT	LAN led active blinking	I/O	3.3V	
203	GPIO4_6	GPIO	I/O	3.3V	
204	LED_LINK	LAN led linking	I/O	3.3V	

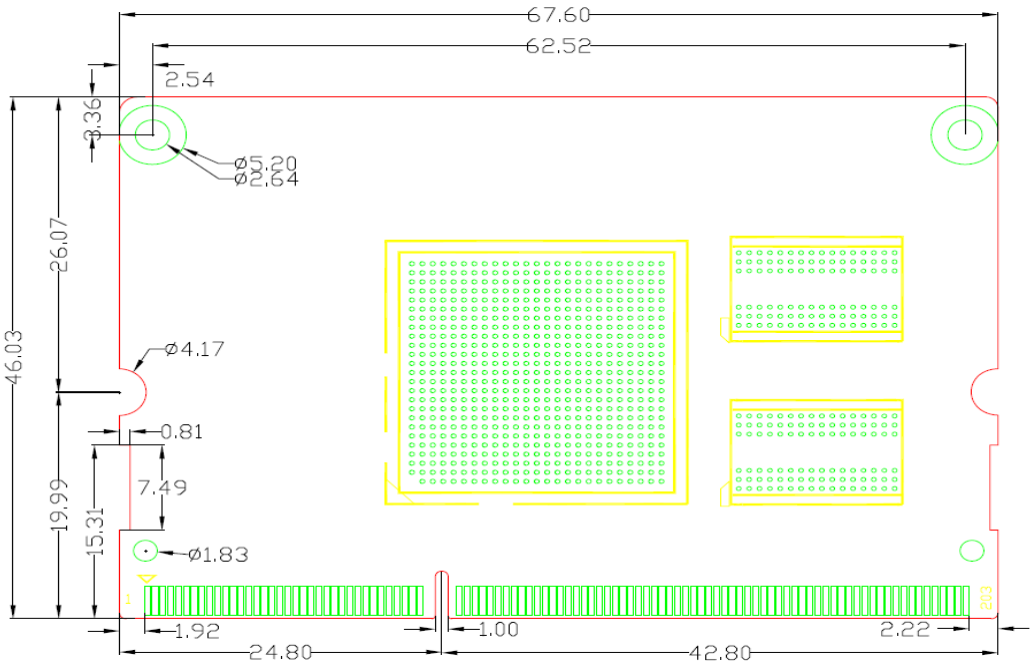
2.3 Technical Specitfications

2.3.1 Electrical Characteristics

Table 2.5.1-1 Absolute Maximum Ratings

Symbol	Description	Input/Output	Min	Type	Max	Unit
5VIN	Main power supply	Input	-0.3	5	5.5	V
Ivbat	Main power current	input	180	300	500	mA
3P3V	Digital power supply	Output	-0.3	3.3	3.6	V
VDD_RTC	RTC power supply	Input	-0.3	3.1	3.3	V
2P5V	Digital power supply	Output	-0.3	2.5	2.75	V
OTG_VBUS	USB OTG power supply	Input	-0.5	5.0	5.25	V
RGMII_VDD2V5	LAN power supply	Output	-0.3	2.5	2.75	V
VCC_1P2V	CPU core power supply	Output	-0.3	1.2	1.32	V
DDR_1_5V	DDR power supply	Output	-0.3	1.5	1.65	V

2.3.2 Mechanical Characteristics



Unit : mm

2.3.3 Thermal Characteristics

Series	Vera Dual	Vera Dual	Vera Quad	Vera Quad
Part Code	VRAD0011	VRAD0021	VRAQ0021	VRAQ0011
Storage Temperature	-40° to 85° C	-40° to 85° C	-40° to 85° C	-40° to 85° C
Operating temperature	0° to 70° C	0° to 70° C	0° to 70° C	0° to 70° C

Technical Support and Warranty

Technical Support

MAS Elettronica provides its product with one-year free technical support including:

- Providing software and hardware resources related to the embedded products of MAS Elettronica;
- Helping customers properly compile and run the source code provided by MAS Elettronica;
- Providing technical support service if the embedded hardware products do not function properly under the circumstance that customers operate according to the instructions in the documents provided by MAS Elettronica;
- Helping customers troubleshoot the products.

The following conditions will not be covered by our technical support service. We will take appropriate measures accordingly:

- Customers encounter issues related to software or hardware during their development process;
- Customers encounter issues caused by any unauthorized alter to the embedded operating system;
- Customers encounter issues related to their own applications;
- Customers encounter issues caused by any unauthorized alter to the source code provided by MAS Elettronica;

Warranty Conditions

1) 12-month free warranty on the PCB under normal conditions of use since the sales of the product;

2) The following conditions are not covered by free services; MAS Elettronica will charge accordingly:

A. Customers fail to provide valid purchase vouchers or the product identification tag is damaged, unreadable, altered or inconsistent with the products.

B. Products are damaged caused by operations inconsistent with the user manual;

C. Products are damaged in appearance or function caused by natural disasters (flood, fire, earthquake, lightning strike or typhoon) or natural aging of components or other force majeure;

D. Products are damaged in appearance or function caused by power failure, external forces, water, animals or foreign materials;

E. Products malfunction caused by disassembly or alter of components by customers or, products disassembled or repaired by persons or organizations unauthorized by MAS Elettronica, or altered in factory specifications, or configured or expanded with the components that are not provided or recognized by MAS Elettronica and the resulted damage in appearance or function;

F. Product failures caused by the software or system installed by customers or inappropriate settings of software or computer viruses;

G. Products purchased from unauthorized sales;

H. Warranty (including verbal and written) that is not made by MAS Elettronica and not included in the scope of our warranty should be fulfilled by the party who committed. MAS Elettronica has no any responsibility;

3) Within the period of warranty, the freight for sending products from customers to Goembed Technology should be paid by customers; the freight from MAS Elettronica to customers should be paid by us. The freight in any direction occurs after warranty period should be paid by customers.

4) Please contact technical support if there is any repair request.

Note:

🕮 MAS Elettronica will not take any responsibility on the products sent back without the permission of the company.

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