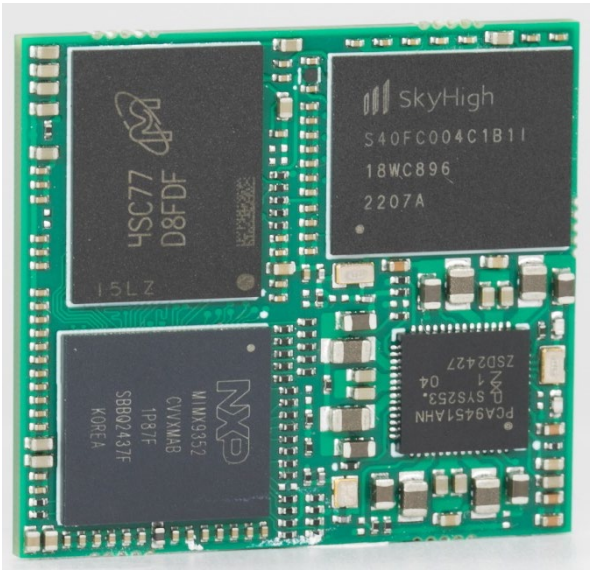
OPEN STANDARD MODULE™

NEITH

i.MX93xx

Hardware Manual



Revision History:

Doc. Version	ANITA Version	Date	Change
V1.0	REV1	2025-01-20	Initial Version

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Introduction

1.1 The OSM Formfactor

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.
The NEITH-IMX93 is based on the new OSM 1.1 standard (Size-S) “Small” for completely machine processible low-cost embedded computer modules during soldering, assembly and testing. Highly scalable and equipped with i.MX 93 Applications Processors manufactured by NXP. The processors integrate ARM Cortex-A55 cores, bringing performance and energy efficiency to Linux-based edge applications and the ARM Ethos-U65 microNPU, enabling developers to create more capable, cost-effective and energy-efficient machine learning (ML) applications. The i.MX 93 processors deliver advanced security with integrated EdgeLock secure enclave and an efficient 2D graphics processing unit (GPU).
MSC OSM-SF-IMX93 provides fast and low power LPDDR4 memory technology with inline ECC support, combined with up to 256GB eMMC Flash memory. Various interfaces for embedded applications such as Dual Gigabit Ethernet (RGMII), USB 2.0, 2x CAN-FD, MIPI-DSI and MIPI CSI-2 (2-lane) for connecting a camera are available. The typical design power ranges from 500mW to 2W.
The module is compliant with the new OSM 1.1 standard (OSM-SF). For evaluation and design-in of the new NEITH-IMX93 module, MSC provides a development platform and a starter kit. A Yocto based Linux Board Support Package is available (Android support on request).

OSM module and carrier specifications are available online at: https://sget.org/standards/osm/

2 Specifications

2.1 Core System

SoC

NXP i.MX 93 ARM Cortex-A55 Applications Processors
- i.MX 9352, dual-core, NPU, 1.7GHz
- i.MX 9332, dual-core, 1.7GHz
- i.MX 9351, single-core, NPU, 1.7GHz
- i.MX 9331, single-core, 1.7GHz
- i.MX 9302, dual-core, 900 MHz
- i.MX 9301, single-core, 900 MHz

Two Cortex®-A55 processors operating up to 1.7 GHz

• 32 KB L1 Instruction Cache

• 32 KB L1 Data Cache

• 64 KB per-core L2 cache

• Media Processing Engine (MPE) with Arm® NeonTM technology supporting the

Advanced Single Instruction Multiple Data architecture

• Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture

Support of 64-bit Arm® v8.2-A architecture

256 KB cluster L3 cache

Parity/ECC protection on L1 cache, L2 cache, and TLB RAMs

Cortex®-M33 CPU operating up to 250 MHz

• Support FPU

• Support MPU

• Support NVIC

• Support FPB

• Support DWT and ITM

• Two-way set-associative 16 KB System Cache with parity support

• Two-way set-associative 16 KB Code Cache with parity support

• 256 KB tightly coupled memory (TCM)

NPU:
Neural Network performance (256 MACs operating up to 1.0 GHz and 2 OPS/MAC)

• NPU targets 8-bit and 16-bit integer RNN

• Handles 8-bit weights

i.MX 93 Applications Processors Family | NXP Semiconductors

Memory

1GB – 2GB, 16 bit LPDDR4/PLDDR4x up to 1.5Ghz

2.2 Video

IMX93 standard display support consists of 1080P single channel 24-bit Parallel/LVDS and MIPI DSI

no 3D Graphics Processing Unit (GPU)
no Video Processing Unit (VPU)

- PXP 2D accelerator
- LCDIF display
    - MIPI DSI: up to 1920x1200p60
    - LVDS Tx: up to 1366x768p60 or 1280x800p60
    - Parallel display: up to 1366x768p60 or 1280x800p60
- ISI camera interface
    - o MIPI-DPHY CSI Rx PHY and MIPI-CSI Controller compliant to MIPI-DSI specification v1.2 and MIPI-DPHY specification v1.2
    - o Image processing for
        - ▪ One processed camera stream at 1080p30, or
        - ▪ One not processed camera stream (no scaling) at 4kp30 depending on system loading and use case
    - o Image down scaling via decimation and bi-phase filtering
    - o Color space conversion
    - o Interlaced to progressive conversions

2.3 Ethernet

Two Ethernet controllers (capable of simultaneous operation)

- One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588
- One Gigabit Ethernet controller with support for TSN in addition to EEE, Ethernet AVB, and IEEE 1588

2.4 Extension busses

USB

2x USB 2.0 and 1x USB2.0 OTG

UART

1x UART Console with Rx, Tx only
1x UART with 2-wire hand shake
2x UART w/o hand shake

CAN bus

2x CAN interfaces with the following features:
Full implementation of CAN with Flexible data rate (CAN FD) protocol specification and CAN Specification Version 2.0, Part B

- — Standard data frames
- — Extended data frames
- — Data length of 0–64 bytes
- — Content-related addressing

- Compliance with ISO 11898-1:2015 standard
- Flexible message buffers that can be configured to store a payload of 0, 8, 16, 32, or 64 bytes

  Increasing the payload size decreases the number of supported message buffers (see FlexCAN memory partition for CAN FD).

  Message buffers are configurable as receive or transmit, supporting standard and extended messages.
- Individual Receive Mask registers for each message buffer
- Full-featured Legacy RX FIFO with storage capacity for six frames and automatic internal pointer handling with DMA support
- Full-featured Enhanced RX FIFO with storage capacity of 20 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Programmable clock source to CAN Protocol Interface, either peripheral clock or oscillator clock
- Optional general purpose RAM space, using RAM not used by reception or transmission structures
- Listen-Only mode
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority

- Timestamp based on 32-bit free-running timer, with optional external time tick
- Global network time, synchronized by specific message
- Maskable interrupts
- Independence from transmission medium (external transceiver is assumed)
- Short latency time due to arbitration scheme for high-priority messages
- Low-power modes, with programmable wake-up on bus activity
- Transceiver delay compensation when transmitting CAN FD messages at faster data rates
- Management of remote request frames, automatically or by software
- Restriction only to write CAN bit time settings and configuration bits in Freeze mode
- Transmit message buffer status (lowest-priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames

SPI

2 x SPI with the following features:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

I2S

1x I2S interfaces with audio resolution from 16-bits to 32-bits and sample rate up to 384KHz.

The I2S (or I2S) module provides a synchronous audio interface (SAI) that supports full- duplex serial interfaces with frame synchronization such as I2S (see Audio Codec support)

I2C

2x I2C interfaces

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multi-master operation
- Master or Slave operation mode.

GPIO

12x GPIO 1.8V with interrupt.

2.5 System Storage

SDIO

1x SDIO (4-bit) compatible up to version 3.0.

The port is derived from the i.MX8M Plus on-chip MMC/SD/SDIO controller (uSDHC2). uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.1/v5.0/v4.4/v4.41/v4.4/v4.3/v4.2
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to 25 MB/s
- 1-bit or 4-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes
- Dedicated card detection, write protection and Reset signals.

eMMC (8 Bit).

- Soldered on module 8, 16, 32, 64 or 128GB (build option) either standard or -40 to +85C temp range Compatible
- MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
- SD/SDIO 3.01 compliance with 200 MHz SDR signaling to support up to 100 MB/sec

2.6 Boot Modes

Three Module pins allow the Carrier board user to select from eight possible boot devices. Three are Module devices, and four are Carrier devices, and one is a remote device. Below the table from the Hardware specifications 1.1 of the boot modes:

BOOT_SEL1#	BOOT_SEL0#	Boot Source	Boot Device
GND	GND	Carrier	SD-Card
GND	Float	Module	e-MMC
Float	GND	Carrier	SPI-Flash
Float	Float	Module	SPI-Flash

Figure 1 BOOT SEL Selection

2.7 Power

Supply Voltage

4.75 V – 5.25 V

2.8 Mechanical and Environmental

Form Factor

SGET OSM SMALL 1.1

Dimension

OSM small size module, 30mm x 30mm

Operating Temperature

Standard: 0°C to +60°C

Rugged: -20°C to +85°C (optional)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

3 Block Diagram

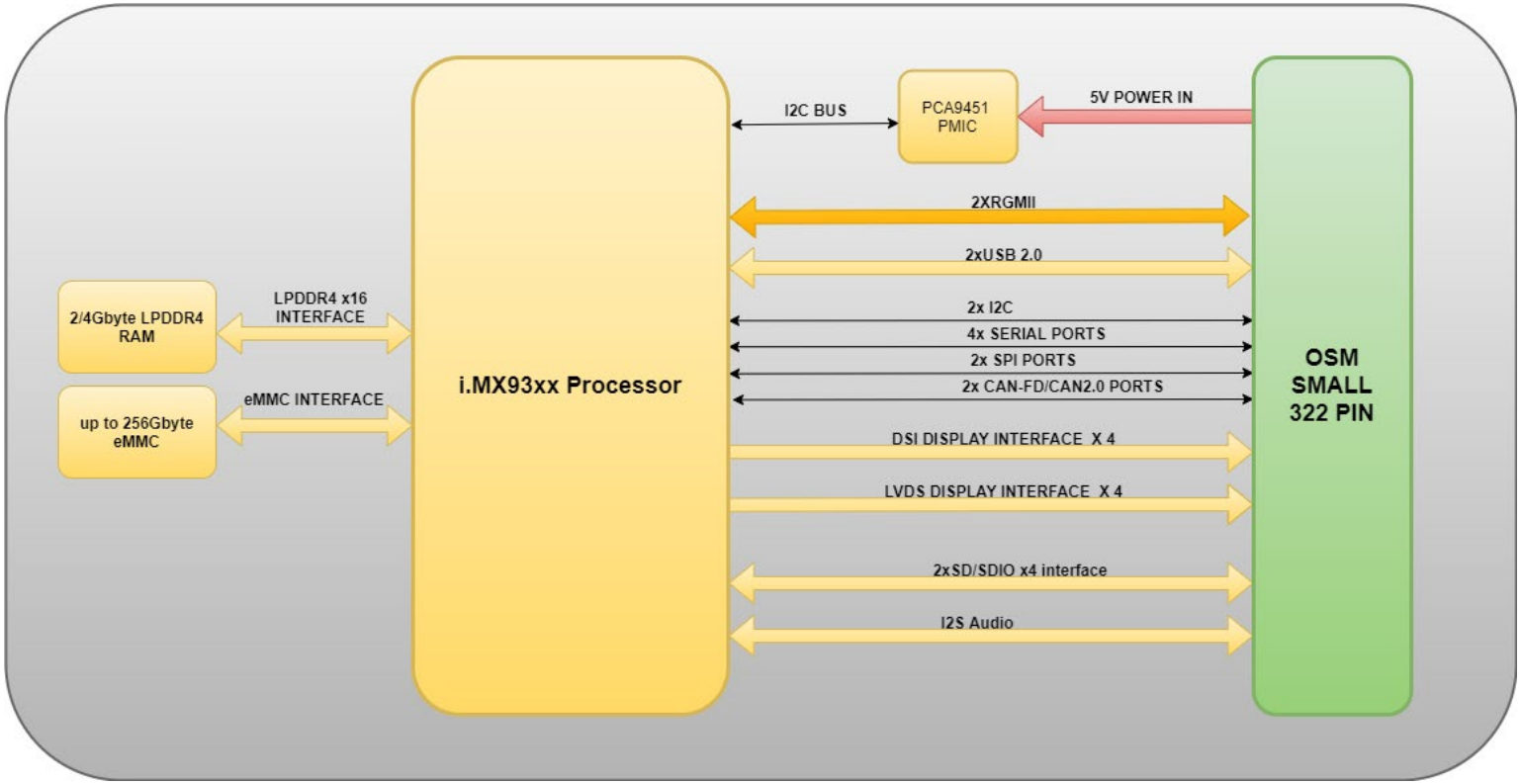
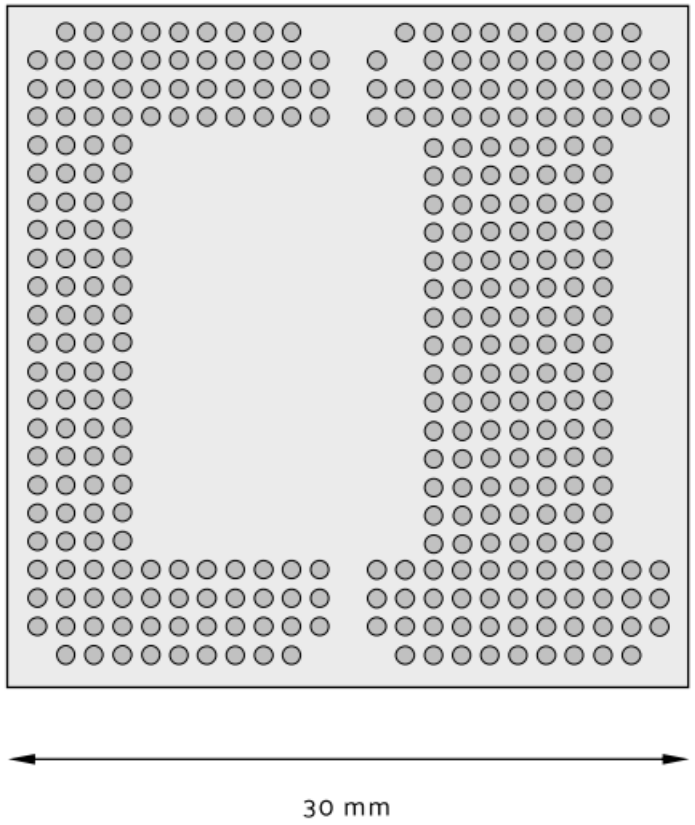


Figure 2 – Module function diagram

4 Pinout and Signal Descriptions

Neith module follows the pinout of the OSM 332 pin Small Form Factor.

The following pages detail what the standard requires, afterwards are illustrated the pinout of the module divided by function and last the mapping of the OSM signals to the with ball of the Processor.



- **Size-0 – "Zero"**: 30 mm x 15 mm / with **188 contacts** → shown below with red outlines
- **Size-S – "Small"**: 30 mm x 30 mm / with **332 contacts** → shown below with blue outlines
- **Size-M – "Medium"**: 30 mm x 45 mm / with **476 contacts** → shown below with orange outlines
- **Size-L – "Large"**: 45 mm x 45 mm / with **662 contacts** → shown below with green outlines

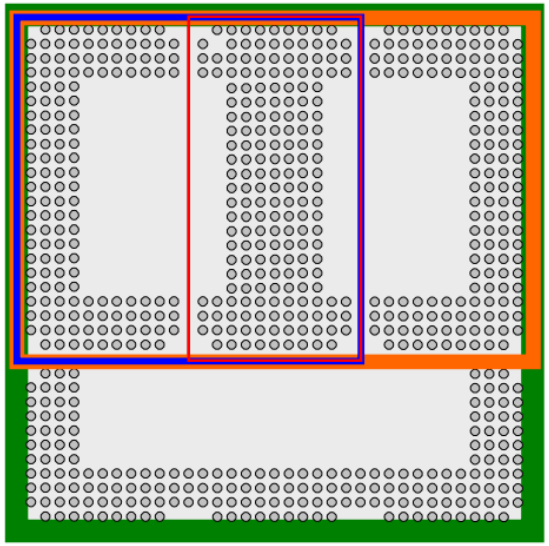
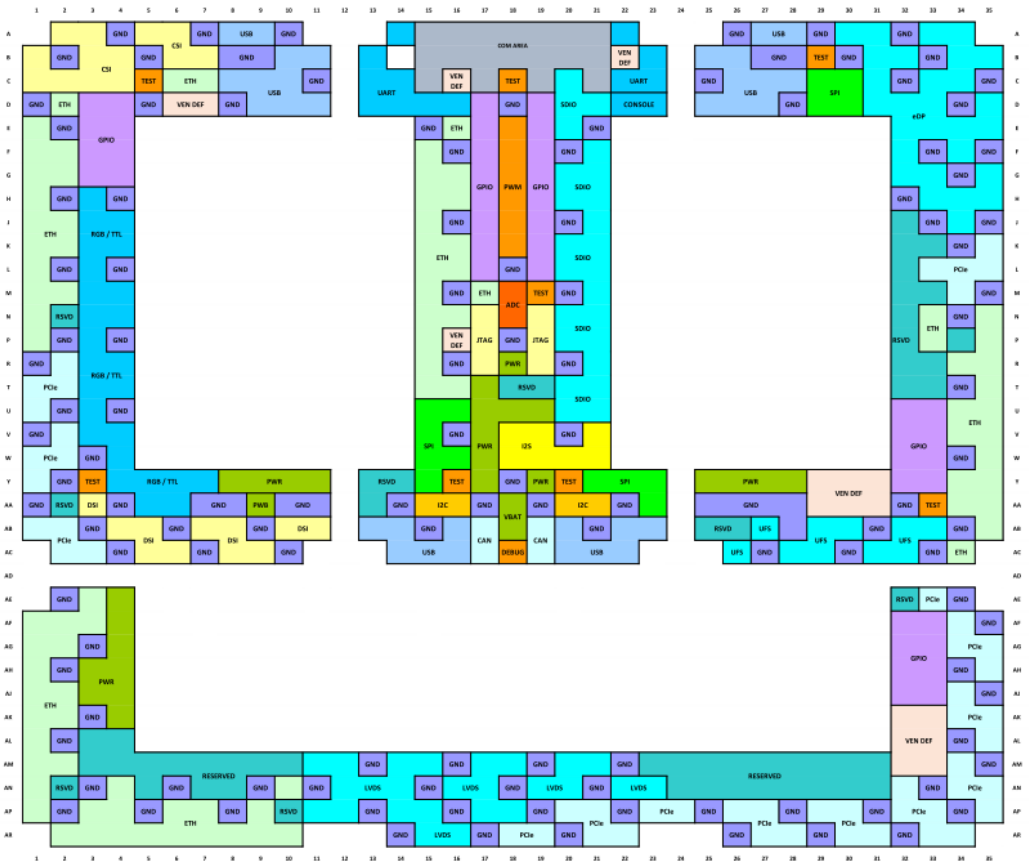


Figure 3 Module Dimentions

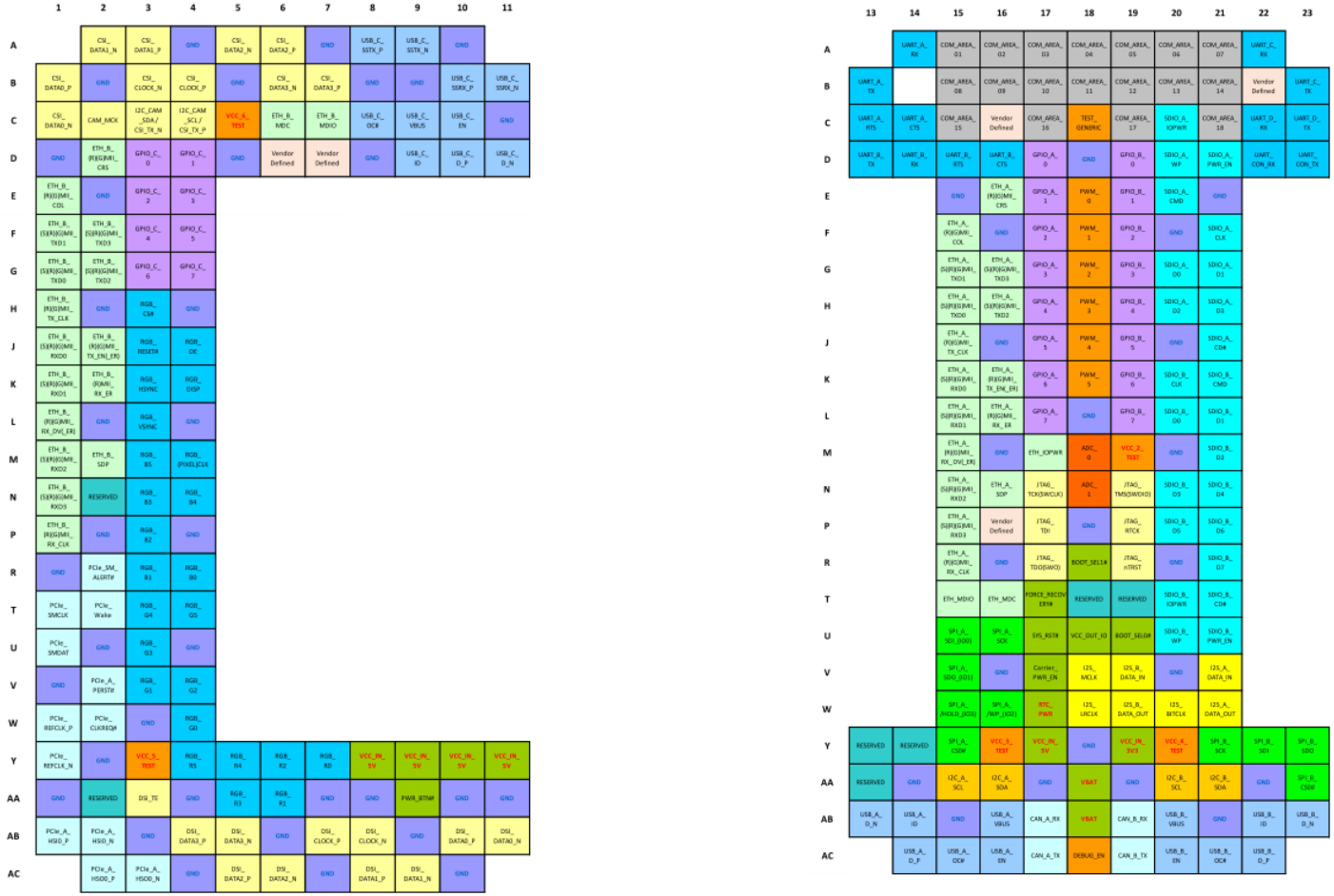


Module Contact Overview

Functionality	Description	Quantity of Interfaces	No. of Contacts	Mandatory Interface	Color Code
Ethernet / LAN	(Q)(S)(R)(G)MII, 100/1000 Mbit	0 … 1	19	No	
USB	USB 2.0	0 … 2	12	No	
UART Console	Rx, Tx only	1 … 2	2	Yes	
UART	Rx, Tx, 2xRTS, 2xCTS	0 … 4	12	No	
Power Supply	5 / 3.3 V-DC, Battery, System Reset, Control signals	1	11	Yes	
Ground	Main Power GND	1	22	Yes	
JTAG		1	6	Yes	
GPIO	General Purpose Input Output	0 … 16	16	No	
Testing	VCC_Test_0 … 3, Debug, etc.	0 … 5	5	No	
Vendor Defined	Defined by module manufacturer	0 … 3	3	No	
Reserved	TBD / for future use	0 … 5	5	No	
Communication Area	Either in Wireless Mode or in Fieldbus Mode	0 … 1	18	No	
SPI	Host or Slave, 1 x Quad SPI optional	0 … 2	10	No	
I2C		0 … 2	4	No	
I2S / PDM	one channel	0 … 2	7	No	
SDIO	4 Lanes + 8 Lanes	0 … 2	24	No	
CAN		0 … 2	4	No	
Analog Input		0 … 2	2	No	
PWM	PWM_0 …5	0 … 6	6	No	
Amount of Contacts			188		

Functionality	Description	Quantity of additional Interfaces	No. of additional Contacts	Mandatory Interface	Color code
Power Supply	5 V-DC, Power Button	1	5	Yes	
Ground	Main Power GND	1	36	Yes	
GPIO	General Purpose Input Output	0 … 8	8	No	
Reserved	TBD / for future use	0 … 2	2	No	
Vendor Defined	Defined by module manufacturer	0 … 2	2	No	
Ethernet / LAN	(Q)(S)(R)(G)MII, 100/1000 Mbit	0 … 1	18	No	
USB	USB 2.0 with 3.0 option, with Dual Role option	0 … 1	10	No	
MIPI Interfaces	DSI, CSI	0 … 3	24	No	
RGB	Parallel Display	0 … 1	25	No	
Testing	VCC_Test_5 … 6	0 … 2	2	No	
PCIe x1	With WAKE and SMBus signal	0 … 1	12	No	
Amount of Contacts			144		

OSM Small Module Contact Overview



OSM Small Module Contact Detail

4.2 Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with mandatory PU (pull up) on module
OD	Open drain
I/O	Bi-directional Input/Output
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module
VDD_IN	Main power source from carrier to module
CMOS	Logic input or output
GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	Low Voltage Differential Signal for DisplayPort interface
LVDS D-PHY	Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays
LVDS M-PHY	Low Voltage Differential Signal for MIPI CSI-3 cameras
LVDS LCD	Low Voltage Differential Signal for LCD displays
LVDS PCIE	Low Voltage Differential Signal for PCIe
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
3.3V	3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)

4.2.1 LVDS0 MODE

NEITH i.MX93 has integrated LVDS interface feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS_TX0_N LVDS_TX0_P LVDS_TX1_N LVDS_TX1_P LVDS_TX2_N LVDS_TX2_P LVDS_TX3_N LVDS_TX3_P	T4 T3 V4 V3 AA6 AA5 Y6 Y7	Primary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
LVDS_CLK_N LVDS_CLK_P	Y5 Y4	Primary LVDS channel differential pair clock lines	O LVDS LCD		Runtime		

4.2.2 DSI MODE (build option)

NEITH i.MX93 has integrated DSI Bridge as a build option. It drives directly a DSI panel without help of other electronics. The following table shows the pins of the OSM connector are used when the DSI feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Do-main	PU / PD	Comments
DSI_D0_N DSI_D0_P DSI_D1_N DSI_D1_P DSI_D2_N DSI_D2_P DSI_D3_N DSI_D3_P	AB11 AB10 AC9 AC8 AC6 AC5 AB5 AB4	Primary DSI panel differential pair data lines	O D-PHY		Runtime		Build option
DSI_CLK_N DSI_CLK_P	AB8 AB7	Primary DSI panel differential pair clock lines.	O D-PHY		Runtime		Build option

4.2.4 MIPI CSI0 (Camera)

NEITH i.MX93 has integrated MIPI-CSI interface with up-to four data lanes and one clock lanes with MIPI D-PHY specification V1.2

The following table shows the pins of the SMARC connector are used when the MIPI CSI feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI_D0_N CSI_D0_P CSI_D1_N CSI_D1_P	C1 B1 A2 A3	CSI0 differential input (point to point)	I.D-PHY		Runtime		
CSI_CLK_N CSI_CLK_P	B3 B4	CSI0 differential clock input (point to point)	I D-PHY		Runtime		
CAM_MCK (CLKO03_GPIO4_27)	C18	Master clock output	O CMOS	1.8V	Runtime		This signal is used by both CSI0 and CSI1

4.2.6 USB 2.0 Ports

NEITH i.MX93 has integrated USB 2.0 OTG controller. The following table shows the pins of the OSM connector.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB1_D_N USB1_D_P	AB23 AC22	USB differential data pairs for port 1	I/O USB	USB	Runtime		From SOC
GPIO_IO13	AC21	USB over-current sense for port 1	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB1_VBUS_3V3	AB20	USB port 1 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Runtime		Can be connected to a USB client port VBUS pin
USB1_ID	AB22	Input pin to an-nounce OTG device insertion on USB 2.0 port	I CMOS	3.3Vsb / 3.3V	Runtime		
GPIO_IO12	AC20	USB Power Enable	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	
USB2_D_N USB2_D_P	AB13 AC14	USB differential data pairs for port 2	I/O USB	USB	Runtime		From SOC

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO_IO15	AC15	USB over-current sense for port 2	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	
USB2_VBUS_3V3	AB16	USB port 1 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Runtime		Can be connected to a USB client port VBUS pin
USB2_ID	AB14	Input pin to announce OTG device insertion on USB 2.0 port	I CMOS	3.3Vsb / 3.3V	Runtime		
GPIO_IO12	AC16	USB Power Enable	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	

4.2.8 LAN Port

NEITH i.MX93 two MAC Interfaces RGMII interface

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ENET1_RD0 ENET1_RD1 ENET1_RD2 ENET1_RD3 ENET1_RX_CTL ENET1_RXC ENET1_TD0 ENET1_TD1 ENET1_TD2 ENET1_TD3 ENET1_TX_CTL ENET1_TXC ENET1_MDC_R ENET1_MDIO_R	J1 K1 M1 N1 L1 P1 G1 F1 G2 F2 J2 H1 C6 C7	Gigabit Ethernet Controller 1: Media Dependent RGMII	GBE RGMII		Runtime		Direct RGMII MAC 1 Interface..
ENET2_MDC_R ENET2_MDIO_R ENET2_RD0 ENET2_RD1 ENET2_RD2 ENET2_RD3	T16 T15 K15 L15 N15 P15	Gigabit Ethernet Controller 2 Media Dependent RGMII	GBE RGMII		Runtime		Direct RGMII MAC 2 Interface..

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ENET2_RX_CTL	M15						
ENET2_RXC	R15						
ENET2_TD0	H15						
ENET2_TD1	G15						
ENET2_TD2	H16						
ENET2_TD3	G16						
ENET2_TX_CTL	K16						
ENET2_TXC	J15						

4.2.9 SDIO Port

NEITH i.MX93 has Two MMC/SD/SDIO port. The port is derived from the i.MX8M Mini on-chip MMC/SD/SDIO controller (uSDHC2)

The following table shows the pins of the SMARC connector are used when the SDIO feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SD2_DATA0 SD2_DATA1 SD2_DATA2 SD2_DATA3	G20 G21 H20 H21	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will de-tect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SD2_CMD	E20	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SD2_nCD	J21	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SD2_CLK	F21	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SD3_DATA0 SD3_DATA1 SD3_DATA2 SD3_DATA3	L20 L21 M21 N20	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SD3_CMD	K21	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
		During command transfer this signal is in push-pull mode.					
SD3_CLK	K20	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		

4.2.10 SPI1/SPI6 Port

NEITH i.MX93 module supports two SPI port. Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
lpspi1_pcs0	Y15	SPI1 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
lpspi1_sck	U16	SPI1 Clock	O CMOS	1.8V	Standby		SPI1 CLOCK
lpspi1_sin	U15	SPI1 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
lpspi1_sout	V15	SPI1 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
lpspi6_pcs0	AA23	SPI6 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
lpspi6_sck	Y21	SPI6 Clock	O CMOS	1.8V	Standby		SPI6 CLOCK
lpspi6_sin	Y22	SPI6 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
lpspi6_sout	Y23	SPI6 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

4.2.12 I2C interfaces

NEITH i.MX93 module supports 3 I2C interfaces:

Most of the other I2C busses are described in their designated function tables rather than in a single big list.

Below is an overview of all I2C busses and where to find them.

Name	Pin #	Description	Comments
I2C1_DAT	AA16	I2C1 data line	3V3 signal level
I2C1_CK	AA15	I2C1 clock line	3V3 signal level
I2C2_DAT	AA21	I2C2 data line	3V3 signal level
I2C2_CK	AA20	I2C2 clock line	3V3 signal level
I2C5_DAT	F3	I2C5 data line	3V3 signal level
I2C5_CK	F4	I2C5 clock line	3V3 signal level

4.2.13 General purpose I/O (GPIO)

NEITH i.MX93 module supports.

The following table shows the pins of the OSM connector are used when the GPIO feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO_A_0	D17	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module.	GPIO_IO24
GPIO_A_1	E17	General purpose I/O pin 1.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO25
GPIO_A_2	F17	General purpose I/O pin 2.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO26
GPIO_A_3	G17	General purpose I/O pin 3.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO27
GPIO_A_4	H17	General purpose I/O pin 4.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO28
GPIO_A_5	J17	General purpose I/O pin 5.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	PDM_DATA1(gpio1_10)
GPIO_A_6	K17	General purpose I/O pin 6.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	CLKO01(gpio3_26)
GPIO_A_7	L17	General purpose I/O pin 7.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	CLKO02(gpio3_27)
GPIO_C_0	D3	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO18

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO_C_1	D4	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO17
GPIO_C_2	E3	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO16
GPIO_C_3	E4	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO22(lpi2c5_sda)
GPIO_C_4	F3	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO23(lpi2c5_scl)
GPIO_C_5	F4	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO21
GPIO_C_6	G3	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO20
GPIO_C_7	G4	General purpose I/O pin 0.	I/O CMOS	3,3V/1.8V	Runtime	PU 470K on the Module	GPIO_IO19

4.2.14 UART

NEITH i.MX93 module supports.supports 4 universal asynchronous receiver/transmitter (UART) .

The following table shows the pins of the OSM connector are used when the UART feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
UART1_RXD	D22	Asynchronous serial data input port 1	I CMOS	3,3V/1.8V	Runtime		
UART1_TXD	D23	Asynchronous serial data output port 1	OI CMOS	3,3V/1.8V	Runtime		
UART2_RXD	A22	Asynchronous serial data input port 2	I CMOS	3,3V/1.8V	Runtime		
UART2_TXD	B23	Asynchronous serial data output port 2	O CMOS	3,3V/1.8V	Runtime		
lpuart6_tx	B13	Asynchronous serial data output port 6	O CMOS	3,3V/1.8V	Runtime		
lpuart6_rx	A14	Asynchronous serial data input port 6	I CMOS	3,3V/1.8V	Runtime		
lpuart6_cts	C14	Asynchronous serial clear to send port 6	O CMOS	3,3V/1.8V	Runtime		
lpuart6_rts	C13	Asynchronous serial request to send port 6	I CMOS	3,3V/1.8V	Runtime		
lpuart7_tx	D13	Asynchronous serial data output port 7	O CMOS	3,3V/1.8V	Runtime		

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
lpuart7_rx	D14	Asynchronous serial data input port 7	I CMOS	3,3V/1.8V	Runtime		
lpuart7_cts	D16	Asynchronous serial clear to send port 7	O CMOS	3,3V/1.8V	Runtime		
lpuart7_rts	D15	Asynchronous serial request to send port 7	I CMOS	3,3V/1.8V	Runtime		

4.2.14 CAN BUS

NEITH i.MX93 module 2 CAN Flexible data rate (CAN FD) protocol specification and CAN Specification Version 2.0, Part B

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN2_TX	E17	CAN port 2 Transmit output	O CMOS	3.3V	Runtime		
CAN2_RX	G17	CAN port 2 Receive input	I CMOS	3.3V	Runtime		
CAN1_TX	AC17	CAN port 1 Transmit output	O CMOS	3.3V	Runtime		
CAN1_RX	AB17	CAN port1 Receive input	I CMOS	3.3V	Runtime		

4.2.16 Power and System Management and MISC

The following table shows the pins of the SMARC connector are used when the Power and System Management feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
RESET_IN#	U17	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
ADC_0	M18	ADC IN 0	I ANA-LOG	1.8V	Runtime		Range 0 to 1,8V
ADC_1	N18	ADC IN 1	I ANA-LOG	1.8V	Runtime		Range 0 to 1,8V
ADC_2	C16	ADC IN 2	I ANA-LOG	1.8V	Runtime		Range 0 to 1,8V
ADC_3	B22	ADC IN 3	I ANA-LOG	1.8V	Runtime		Range 0 to 1,8V

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
TAMPER 0	D7	TAMPER INPUT 0	I CMOS	1.8V	Runtime		
TAMPER 1	D6	TAMPER INPUT 1	I CMOS	1.8V	Runtime		

4.2.17 Boot Select

The following table shows the pins of the OSM connector are used when the Boot selection.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# **BOOT_SEL1#**	U19 R18	Input straps determine the Module boot	I OD CMOS	1.8Vsb	Standby	PU 4.7K	Driven by OD on Carrier. Pulled up on module. Booting from EMMc and SDcard is supported

4.2.17 Power

The following table shows the pins of the SMARC connector are used for the power supply of the board.

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VCC_IN_5V	Y8, Y9, Y10, Y11, Y17	Module power input voltage 4.75 min to 5.25V max	P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?	3 to 5.25V / 5V		
GND	D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21, A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10	Module signal and power return, and GND reference	P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?	Ground		
RTC_PWR	W17	RTC 3V POWER INPUT				

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VCC_OUT_IO	U18	VCC OUT FOR IO ON CARRIER	OUT PWR	3V3		3V3 OUT FOR IO.
SDIO_A_PWR	C20	POWER FOR SDIO CHANNEL 2 uSD	OUT PWR	1V8/3V3		
SDIO_B_PWR	T20	POWER FOR SDIO CHANNEL 3 SDIO	OUT PWR	1V8/3V3		
ETH_IO_PWR	M17	POWER FOR ETH IO INTERFACE	OUT PWR	1V8/3V3		

TEST_VOLTAGES

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VCC_2_TEST	M19	LPD4/x_VDDQ_0V6	POWER OUT			0,6V LPDDR4x POWER
VCC_3_TEST	Y16	LPD4/x_VDD2_1V1	POWER OUT			1,1V LPDDR4x POWER

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VCC_4_TEST	Y20	VDD_1V8	POWER OUT			1,8V module power out
VCC_5_TEST	Y3	NVCC_BBSM_1V8	POWER OUT			1,8V BBSM POWER
VCC_6_TEST	C5	VDD_SOC_0V85	POWER OUT			0,85V CPU Power

5 OSM pin to i.MX93xx mapping

The following table shows the mapping of the i.MX93 pins to the OSM Connector.

PIN Number	Routed pin/signal	Peripheral Selected	Signal Name	Board Signal Name	OSM PIN
W1	[W1] DAP_TDI	JTAG	jtag_mux_tdi	JTAG_TDI	P17
Y1	[Y1] DAP_TCLK_SWCLK	JTAG	jtag_mux_tck	JTAG_TCK	N17
W2	[W2] DAP_TMS_SWDIO	JTAG	jtag_mux_tms	JTAG_TMS	N19
Y2	[Y2] DAP_TDO_TRAC-ESWO	JTAG	jtag_mux_tdo	JTAG_TDO	R17
AA2	[AA2] CCM_CLKO1	GPIO3	gpio_io, 26	GPIO3_26	K17
Y3	[Y3] CCM_CLKO2	GPIO3	gpio_io, 27	GPIO3_27	L17
AA3	[AA3] ENET2_RXC	ENET1	enet_rx_er	ENET2_RXC	R15
U4	[U4] CCM_CLKO3	GPIO4	gpio_io, 28	GPIO4_28	C18
V4	[V4] CCM_CLKO4	GPIO4	gpio_io, 29	GPIO4_29	P16
Y4	[Y4] ENET2_RX_CTL	ENET1	enet_rgmii_rx_ctl	ENET2_RX_CTL	M15
AA4	[AA4] ENET2_RD0	ENET1	enet_rgmii_rd, 0	ENET2_RD0	K15
Y5	[Y5] ENET2_RD1	ENET1	enet_rgmii_rd, 1	ENET2_RD1	L15
AA5	[AA5] ENET2_RD2	ENET1	enet_rgmii_rd, 2	ENET2_RD2	N15
U6	[U6] ENET2_TXC	ENET1	enet_rgmii_txc	ENET2_TXC	J15
V6	[V6] ENET2_TX_CTL	ENET1	enet_rgmii_tx_ctl	ENET2_TX_CTL	K16
Y6	[Y6] ENET2_RD3	ENET1	enet_rgmii_rd, 3	ENET2_RD3	P15

AA6	[AA6] ENET2_MDIO	ENET1	enet_mdio	ENET2_MDIO	P15
Y7	[Y7] ENET2_MDC	ENET1	enet_mdc	ENET2_MDC	T16
AA7	[AA7] ENET1_RXC	ENET_QOS	enet_qos_rx_er	ENET1_RXC	P1
T8	[T8] ENET2_TD0	ENET1	enet_rgmii_td, 0	ENET2_TD0	G1
U8	[U8] ENET2_TD1	ENET1	enet_rgmii_td, 1	ENET2_TD1	F1
V8	[V8] ENET2_TD2	ENET1	enet_rgmii_td, 2	ENET2_TD2	G2
Y8	[Y8] ENET1_RX_CTL	ENET_QOS	enet_qos_rgmii_rx_ctl	ENET1_RX_CTL	L1
AA8	[AA8] ENET1_RD0	ENET_QOS	enet_qos_rgmii_rd, 0	ENET1_RD0	J1
Y9	[Y9] ENET1_RD1	ENET_QOS	enet_qos_rgmii_rd, 1	ENET1_RD1	K1
AA9	[AA9] ENET1_RD2	ENET_QOS	enet_qos_rgmii_rd, 2	ENET1_RD2	M1
T10	[T10] ENET2_TD3	ENET1	enet_rgmii_td, 3	ENET2_TD3	F2
U10	[U10] ENET1_TXC	ENET_QOS	enet_qos_tx_er	ENET1_TXC	H1
V10	[V10] ENET1_TX_CTL	ENET_QOS	enet_qos_rgmii_tx_ctl	ENET1_TX_CTL	J2
Y10	[Y10] ENET1_RD3	ENET_QOS	enet_qos_rgmii_rd, 3	ENET1_RD3	N1
AA10	[AA10] ENET1_MDIO	ENET_QOS	enet_qos_mdio	ENET1_MDIO	C7
W11	[W11] ENET1_TD0	ENET_QOS	enet_qos_rgmii_td, 0	ENET1_TD0	G1
Y11	[Y11] SD1_CLK	USDHC1	usdhc_clk	SD1_CLK	INT
AA11	[AA11] ENET1_MDC	ENET_QOS	enet_qos_mdc	ENET1_MDC	C6
T12	[T12] ENET1_TD1	ENET_QOS	enet_qos_rgmii_td, 1	ENET1_TD1	F1
U12	[U12] ENET1_TD2	ENET_QOS	enet_qos_rgmii_td, 2	ENET1_TD2	G2
V12	[V12] ENET1_TD3	ENET_QOS	enet_qos_rgmii_td, 3	ENET1_TD3	F2
Y12	[Y12] SD1_STROBE	USDHC1	usdhc_strobe	SD1_STROBE	INT
AA12	[AA12] SD1_CMD	USDHC1	usdhc_cmd	SD1_CMD	INT
Y13	[Y13] SD1_DATA4	USDHC1	usdhc_data, 4	SD1_DATA4	INT
AA13	[AA13] SD1_DATA3	USDHC1	usdhc_data, 3	SD1_DATA3	INT

T14	[T14] SD3_DATA3	USDHC3	usdhc_data, 3	SD3_DATA3	N20
U14	[U14] SD3_DATA2	USDHC3	usdhc_data, 2	SD3_DATA2	M21
V14	[V14] SD3_DATA1	USDHC3	usdhc_data, 1	SD3_DATA1	L21
Y14	[Y14] SD1_DATA5	USDHC1	usdhc_data, 5	SD1_DATA5	INT
AA14	[AA14] SD1_DATA0	USDHC1	usdhc_data, 0	SD1_DATA0	INT
Y15	[Y15] SD1_DATA6	USDHC1	usdhc_data, 6	SD1_DATA6	INT
AA15	[AA15] SD1_DATA1	USDHC1	usdhc_data, 1	SD1_DATA1	INT
T16	[T16] SD3_DATA0	USDHC3	usdhc_data, 0	SD3_DATA0	L20
U16	[U16] SD3_CMD	USDHC3	usdhc_cmd	SD3_CMD	K21
V16	[V16] SD3_CLK	USDHC3	usdhc_clk	SD3_CLK	K20
Y16	[Y16] SD1_DATA7	USDHC1	usdhc_data, 7	SD1_DATA7	INT
AA16	[AA16] SD1_DATA2	USDHC1	usdhc_data, 2	SD1_DATA2	INT
G17	[G17] PDM_CLK	CAN1	can_tx	can1_tx	AC17
J17	[J17] PDM_BIT_STREAM0	CAN1	can_rx	can1_rx	AB17
L17	[L17] GPIO_IO04	LPUART6	lpuart_tx	lpuart6_tx	B13
N17	[N17] GPIO_IO10	LPUART7	lpuart_cts_b	lpuart7_cts_b	D16
R17	[R17] GPIO_IO19	GPIO2	gpio_io, 19	GPIO_IO19	G4
Y17	[Y17] SD2_CD_B	USDHC2	usdhc_cd_b	SD2_CD_B	J21
G18	[G18] PDM_BIT_STREAM1	GPIO1	gpio_io, 10	GPIO1_IO10	J17
J18	[J18] WDOG_ANY	WDOG1	wdog_wdog_any	wdog_wdog_any	INT
L18	[L18] GPIO_IO05	LPUART6	lpuart_rx	lpuart6_rx	A14
N18	[N18] GPIO_IO11	LPUART7	lpuart_rts_b	lpuart7_rts_b	D15
R18	[R18] GPIO_IO18	GPIO2	gpio_io, 18	GPIO_IO18	D3
U18	[U18] GPIO_IO22	LPI2C5	lpi2c_sda	lpi2c5_sda	F3

V18	[V18] SD2_VSELECT	USDHC2	usdhc_vselect	SD2_VSELECT	INT
Y18	[Y18] SD2_DATA0	USDHC2	usdhc_data, 0	SD2_DATA0	G20
AA18	[AA18] SD2_DATA1	USDHC2	usdhc_data, 1	SD2_DATA1	G21
Y19	[Y19] SD2_CMD	USDHC2	usdhc_cmd	SD2_CMD	E20
AA19	[AA19] SD2_CLK	USDHC2	usdhc_clk	SD2_CLK	F21
C20	[C20] I2C1_SCL	LPI2C1	lpi2c_scl	I2C1_SCL	AA15
D20	[D20] I2C2_SCL	LPI2C2	lpi2c_scl	I2C2_SCL	AA20
E20	[E20] UART1_RXD	LPUART1	lpuart_rx	UART1_RXD	D22
F20	[F20] UART2_RXD	LPUART2	lpuart_rx	UART2_RXD	A22
G20	[G20] SAI1_TXC	LPSPI1	lpspi_sin	lpspi1_sin	U15
H20	[H20] SAI1_RXD0	LPSPI1	lpspi_sout	lpspi1_sout	V15
J20	[J20] GPIO_IO01	LPSPI6	lpspi_sin	lpspi6_sin	Y22
K20	[K20] GPIO_IO02	LPSPI6	lpspi_sout	lpspi6_sout	Y23
L20	[L20] GPIO_IO06	LPUART6	lpuart_cts_b	lpuart6_cts_b	C14
M20	[M20] GPIO_IO08	LPUART7	lpuart_tx	lpuart7_tx	D13
N20	[N20] GPIO_IO12	GPIO2	gpio_io, 12	GPIO_IO12	AC20
P20	[P20] GPIO_IO14	GPIO2	gpio_io, 14	GPIO_IO14	AC16
R20	[R20] GPIO_IO17	GPIO2	gpio_io, 17	GPIO_IO17	D4
T20	[T20] GPIO_IO20	GPIO2	gpio_io, 20	GPIO_IO20	G3
U20	[U20] GPIO_IO23	LPI2C5	lpi2c_scl	lpi2c5_scl	E4
V20	[V20] GPIO_IO26	GPIO2	gpio_io, 26	GPIO_IO26	F17
W20	[W20] GPIO_IO28	GPIO2	gpio_io, 28	GPIO_IO28	H17
Y20	[Y20] SD2_DATA2	USDHC2	usdhc_data, 2	SD2_DATA2	H20
AA20	[AA20] SD2_DATA3	USDHC2	usdhc_data, 3	SD2_DATA3	H21
C21	[C21] I2C1_SDA	LPI2C1	lpi2c_sda	I2C1_SDA	AA16

D21	[D21] I2C2_SDA	LPI2C2	lpi2c_sda	I2C2_SDA	AA21
E21	[E21] UART1_TXD	LPUART1	lpuart_tx	UART1_TXD	D23
F21	[F21] UART2_TXD	LPUART2	lpuart_tx	UART2_TXD	B23
G21	[G21] SAI1_TXFS	LPSPI1	lpspi_pcs, 0	lpspi1_pcs_0	Y15
H21	[H21] SAI1_TXD0	LPSPI1	lpspi_sck	lpspi1_sck	U16
J21	[J21] GPIO_IO00	LPSPI6	lpspi_pcs, 0	lpspi6_pcs_0	AA23
K21	[K21] GPIO_IO03	LPSPI6	lpspi_sck	lpspi6_sck	Y21
L21	[L21] GPIO_IO07	LPUART6	lpuart_rts_b	lpuart6_rts_b	C13
M21	[M21] GPIO_IO09	LPUART7	lpuart_rx	lpuart7_rx	D14
N21	[N21] GPIO_IO13	GPIO2	gpio_io, 13	GPIO_IO13	AC21
P21	[P21] GPIO_IO15	GPIO2	gpio_io, 15	GPIO_IO15	AC15
R21	[R21] GPIO_IO16	GPIO2	gpio_io, 16	GPIO_IO16	E3
T21	[T21] GPIO_IO21	GPIO2	gpio_io, 21	GPIO_IO21	F4
U21	[U21] GPIO_IO24	GPIO2	gpio_io, 24	GPIO_IO24	D17
V21	[V21] GPIO_IO25	GPIO2	gpio_io, 25	GPIO_IO25	E17
W21	[W21] GPIO_IO27	GPIO2	gpio_io, 27	GPIO_IO27	G17
B19	ADC_IN0			ADC_IN0	M18
A20	ADC_IN1			ADC_IN1	N18
B20	ADC_IN2			ADC_IN2	C16
B21	ADC_IN3			ADC_IN3	B22
A3	LVDS_CLK_N			LVDS_CLK_N	Y5
B3	LVDS_CLK_P			LVDS_CLK_P	Y4
A5	LVDS_TX0_N			LVDS_TX0_N	T4
B5	LVDS_TX0_P			LVDS_TX0_P	T3
A4	LVDS_TX1_N			LVDS_TX1_N	V4
B4	LVDS_TX1_P			LVDS_TX1_P	V3

A2	LVDS_TX2_N			LVDS_TX2_N	AA6
B2	LVDS_TX2_P			LVDS_TX2_P	AA5
D6	DSI_CLK_N			DSI_CLK_N	AB8
E6	DSI_CLK_P			DSI_CLK_P	AB7
A6	DSI_D0_N			DSI_D0_N	AB11
B6	DSI_D0_P			DSI_D0_P	AB10
A7	DSI_D1_N			DSI_D1_N	AC9
B7	DSI_D1_P			DSI_D1_P	AC8
A8	DSI_D2_N			DSI_D2_N	AC6
B8	DSI_D2_P			DSI_D2_P	AC5
A9	DSI_D3_N			DSI_D3_N	AB5
B9	DSI_D3_P			DSI_D3_P	AB4
D10	CSI_CLK_N			CSI_CLK_N	B3
E10	CSI_CLK_P			CSI_CLK_P	B4
A11	CSI_D0_N			CSI_D0_N	C1
B11	CSI_D0_P			CSI_D0_P	B1
A10	CSI_D1_N			CSI_D1_N	A2
B10	CSI_D1_P			CSI_D1_P	A3

6 Module Outline – 30 mm x 30 mm Module

The Figure 2 on the following page details the 30 mm x 30 mm NEITH OSM mechanical attributes, including the pin numbering and edge finger pattern.

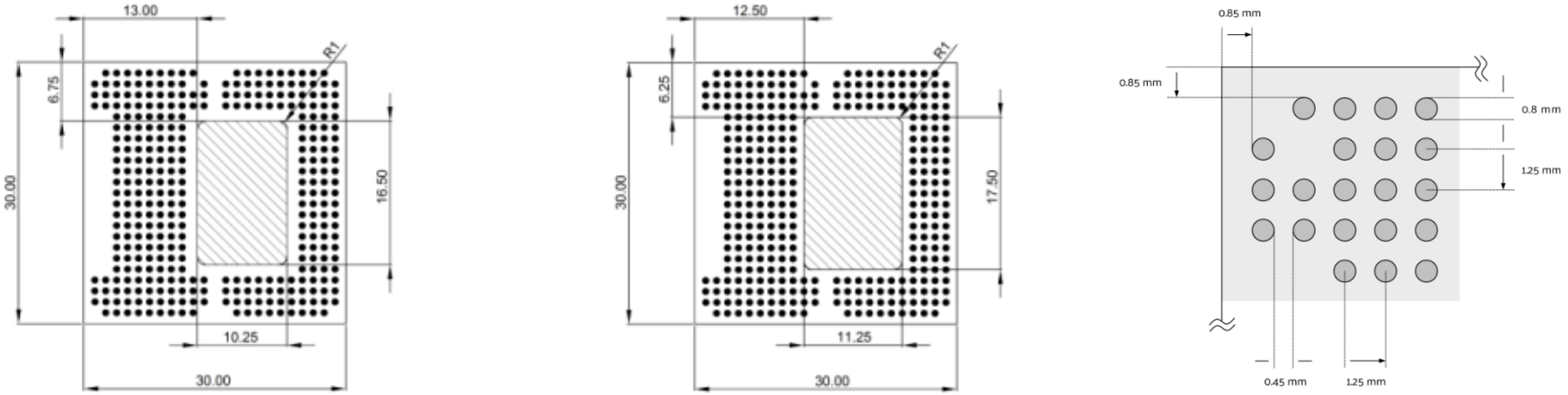


Figure 4 Module pitch and OSM Small dimentions

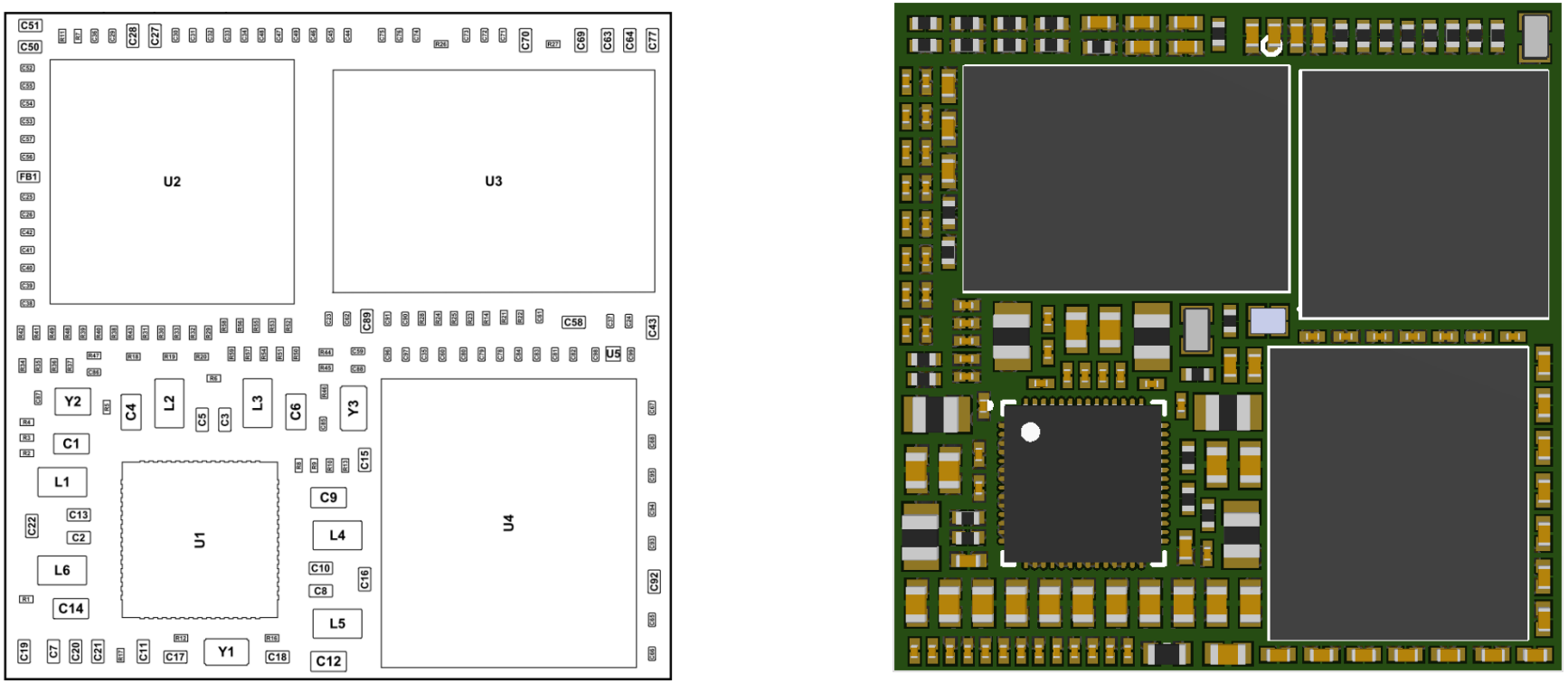


Figure 5 Module Layout on OSM Small dimentions

Technical Support and Warranty

Technical Support

MAS Elettronica provides its product with one-year free technical support including:

1. Providing software and hardware resources related to the embedded products of MAS Elettronica;
2. Helping customers properly compile and run the source code provided by MAS Elettronica;
3. Providing technical support service if the embedded hardware products do not function properly under the circumstance that customers operate according to the instructions in the documents provided by MAS Elettronica;
4. Helping customers troubleshoot the products.

T he following conditions will not be covered by our technical support service. We will take appropriate measures accordingly:

a. Customers encounter issues related to software or hardware during their development process;
b. Customers encounter issues caused by any unauthorized alter to the embedded operating system;
c. Customers encounter issues related to their own applications;
d. Customers encounter issues caused by any unauthorized alter to the source code provided by MAS Elettronica;

Warranty Conditions

- 12-month free warranty on the PCB under normal conditions of use since the sales of the product;
- The following conditions are not covered by free services; MAS Elettronica will charge accordingly:

Customers fail to provide valid purchase vouchers or the product identification tag is damaged, unreadable, altered or inconsistent with the products.

Products are damaged caused by operations inconsistent with the user manual;

Products are damaged in appearance or function caused by natural disasters (flood, fire, earthquake, lightning strike or typhoon) or natural aging of components or other force majeure;

Products are damaged in appearance or function caused by power failure, external forces, water, animals or foreign materials;

Products malfunction caused by disassembly or alter of components by customers or, products disassembled or repaired by persons or organizations unauthorized by MAS Elettronica, or altered in factory specifications, or configured or expanded with the components that are not provided or recognized by MAS Elettronica and the resulted damage in appearance or function;

Product failures caused by the software or system installed by customers or inappropriate settings of software or computer viruses;

Products purchased from unauthorized sales;

Warranty (including verbal and written) that is not made by MAS Elettronica and not included in the scope of our warranty should be fulfilled by the party who committed. MAS Elettronica has no any responsibility;

3 Within the period of warranty, the freight for sending products from customers to MAS Elettronica should be paid by customers; the freight from MAS Elettronica to customers should be paid by us. The freight in any direction occurs after warranty period should be paid by customers.

4 Please contact technical support if there is any repair request.

Note:

- MAS Elettronica will not take any responsibility on the products sent back without the permission of the company.

Contact Information

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Support: support@maselettronica.com

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