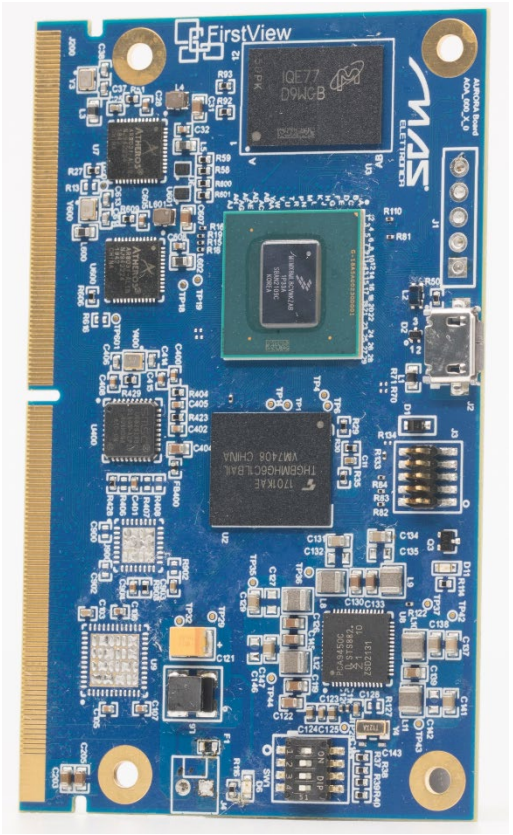
SMARC module

IMX8M Plus

Hardware Manual



Revision History:

Doc. Version	IMX8MP SOM Version	Date	Change
V0.1	REV1.0	2021-09-06	Initial Version
V1.0	REV1.0	2023-04-26	Updated Section 4.3
V1.1	REV1.1	2023-05-17	Updated as per SOM Rev1.1

Introduction

1.1 The SMARC Formfactor

The SMARC (“Smart Mobility ARChitecture”) is a versatile small form factor computer on Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented X86 devices and other RISC CPU’s may be used as well. The Module power envelope is typically under 6W although designs up to about 15W are possible.

Two Module sizes are defined: 82 mm x 50 mm and 82 mm x 80 mm. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5 mm

pitch right angle connector (the connector is sometimes identified as a 321-pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and dual channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

SMARC module and carrier specifications are available online at: https://www.sget.org/standards/smarc.html

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2.0 Specifications

2.1 Core System

SOC:

NXP iMX8M Plus Series

- **i.MX8M Plus Dual** NXP i.MX8M Plus Dual, dual-core ARM Cortex-A53, 1.8GHz
- **i.MX8M Plus Quad Lite** NXP i.MX8M Plus Quad Lite, Quad-core ARM Cortex-A53, 1.8GHz
- **i.MX8M Plus Quad:** NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.6GHz/1.8GHz

  available either as industrial (-40°C to +105°C) or consumer (0°C to +95°C) type"

For more info about the processor NXP:
iMX8M Plus

L2 Cache

512 KB unified L2 cache

Memory

- 1GB – 6GB, LPDDR4 up to 1.5Ghz
- Supports 32-bit LPDDR4-4000 and DDR4-3200

IOT Security (Cybersecurity)

OPTIGA™ TPM SLB 9670 TPM2.0 Infineon Chip.

- Compliant to TPM Main Specification, Family "2.0"
- Random Number Generator (RNG) according to NIST SP800-90°
- Full personalization with Endorsement Key (EK) and EK certificate
- Support of cryptographic algorithms RSA-1028, RSA-2048, ECC NIST P256, ECC BN256, SHA-1, SHA-256
- JEDEC JESD47 industrial qualification

2.2 Video

IMX8M Plus standard display support consists of 1080P capable ePD, single/dual channel 24-bit LVDS and MIPI DSI. The LVDS output is derived from an DSI to LVDS, and the module can output 4-lane DSI.

3D GPU Core:

- Supports OpenGL ES 1.1, 2.0, 3.0,
- OpenCL 1.2, Vulkan
- Trust Zone support using a local MMU to manage secure regions

2D GPU Core:

Multi-pipe 2D raster graphics core that accelerates the 2D graphics display.

LVDS

- LVDS Display Bridge (LDB) supports two channels; each channel has following signals:
- One clock pair and four data pairs.
- One LCDIF drives LVDS Tx, up to 1920x1080p60.

MIPI DSI(Optional)

- MIPI DSI are muxing with LVDS0 signals, in future, we can mount the DNP resistor at processor end.
- Supports one 4-lane MIPI DSI interface operating up to a maximum bit rate of 1.5 Gbps and maximum resolution of 1080p@60fps display output.

Camera support

- Compatible with the MIPI Alliance Interface specification v2.0
- Two MIPI-CSI camera inputs with 4-lane each.

2.3 Ethernet

LAN

SOC embedded with two GbE ETH0 & ETH1 Controller with YT8511H Controller with IEEE-802.3 Supports 10/100/1000Mbps data transfer rates, both full-duplex /half-duplex".

One channel is connected directly to the SoC Ethernet signals, and the second channel is multiplexed with SAI interface.

2.4 Extension busses

PCIe

1x PCI Express (PCIe)

- Single lane supporting PCIe Gen2
- Dual mode operation to function as root complex or endpoint.
- Integrated PHY interface
- Support L1 low power sub-state

USB

4x USB 3.0 /2.0 and, 1x USB3.0 OTG

UART

4x UART interface SER0 (Tx/Rx/CTS/RTS) and SER1(Tx/Rx), SER2(Tx/Rx/CTS/RTS), SER3 (Tx/Rx)

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interruption.

CAN bus

2x CAN interfaces with the following features:

- Implements CAN V2.0B at 1 Mb/s: - 0 to 8-byte length in the data field - Standard and extended data and remote frames.
- Receive Buffers, Masks and Filters: - Two receive buffers with prioritized message storage - Six 29-bit filters - Two 29-bit masks.
- Data Byte Filtering on the First Two Data Bytes (applies to standard data frames)
- Three Transmit Buffers with Prioritization and Abort Features.
- One-Shot mode Ensures Message Transmission is Attempted Only One Time.
- Clock Out Pin with Programmable Prescaler- Can be used as a clock source for other device(s)
- Start-of-Frame (SOF) Signal is Available for Monitoring the SOF Signal: - Can be used for time slot-based protocols and/or bus diagnostics to detect early bus degradation.
- Interrupt Output Pin with Selectable Enables
- Buffer Full Output Pins Configurable as: - Interrupt output for each receiver buffer - General purpose output.

SPI

1 x SPI with the following features:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip-select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

QSPI Support

- Supports one Quad SPI serial flash devices, each with up to four bidirectional data lines. The key features include:
- Each channel can be configured as 1/2/4-bit operation.
- Support both dual-channel or single-channel operation
- Support both SDR mode and DDR mode
- External Memory Overview
- Support up to 166MHz SDR Mode and 166MHz DDR Mode (with external Flash device DQS input)
- Support up to 133MHz SDR Mode and 66MHz DDR Mode (with internal DQS

I2S

2x I2S interfaces with audio resolution from 16-bits to 32-bits and sample rate up to 384KHz.

The I2S (or I2S) module provides a synchronous audio interface (SAI) that supports full- duplex serial interfaces with frame synchronization such as I2S (see Audio Codec support)

I2C

4x I2C interfaces

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multi-master operation
- Master or Slave operation mode.

GPIO

12x GPIO 1.8V with interrupt.

2.5 System Storage

SDIO

1x SDIO (4-bit) compatible up to version 3.0.

The port is derived from the i.MX8M Plus on-chip MMC/SD/SDIO controller (uSDHC2). uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.1/v5.0/v4.4/v4.41/v4.4/v4.3/v4.2
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high capacity SDXC cards up to 2 TB
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to 25 MB/s
- 1-bit or 4-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes
- Dedicated card detection, write protection and Reset signals.

eMMC (8 Bit).

- Soldered on module 8, 16, 32, 64 or 128GB (build option) either standard or -40 to +85C temp range Compatible.
- MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec.
- SD/SDIO 3.01 compliance with 200 MHz SDR signaling to support up to 100 MB/sec.
- Support for SDXC (extended capacity)

EEPROM

- Soldered on module 2Kbit memory (build option) either standard or -40 to +85C temp range Compatible.
- Interfaced with I2C4 bus. Supports 100KHz and 400KHz clock compatibility.
- Is using for storing the Unit Serial ID.

2.6 Boot Modes

Three Module pins allow the Carrier board user to select from eight possible boot devices. Three are Module devices, four are Carrier devices, and one is a remote device. Below the table from the Hardware specifications 2.0 of the boot modes:

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI (CS0#)
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

Figure 1 BOOT SEL Selection

Below is the Boot selection table for the iMX8MPlus Processor, option provided on the SOM board for power ON the standalone SOM.

Boot selection table for the iMX8MP processor				
BOOT_MODE	3	2	1	0
BOOT FROM FUSE	0	0	0	0
SERIAL DOWNLOAD	0	0	0	1
eMMC	0	0	1	0
SD BOOT	0	0	1	1

2.7 Power

Supply Voltage

4.75 V – 5.25 V

2.8 Mechanical and Environmental

Form Factor

SGET SMARC Specifications v2.0/2.1 (2.1 is currently under approval by SGET)

Dimension

SMARC small size module, 82mm x 50mm

Operating Temperature

Standard: 0°C to +60°C

Rugged: -20°C to +85°C (optional)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition

3. Block Diagram

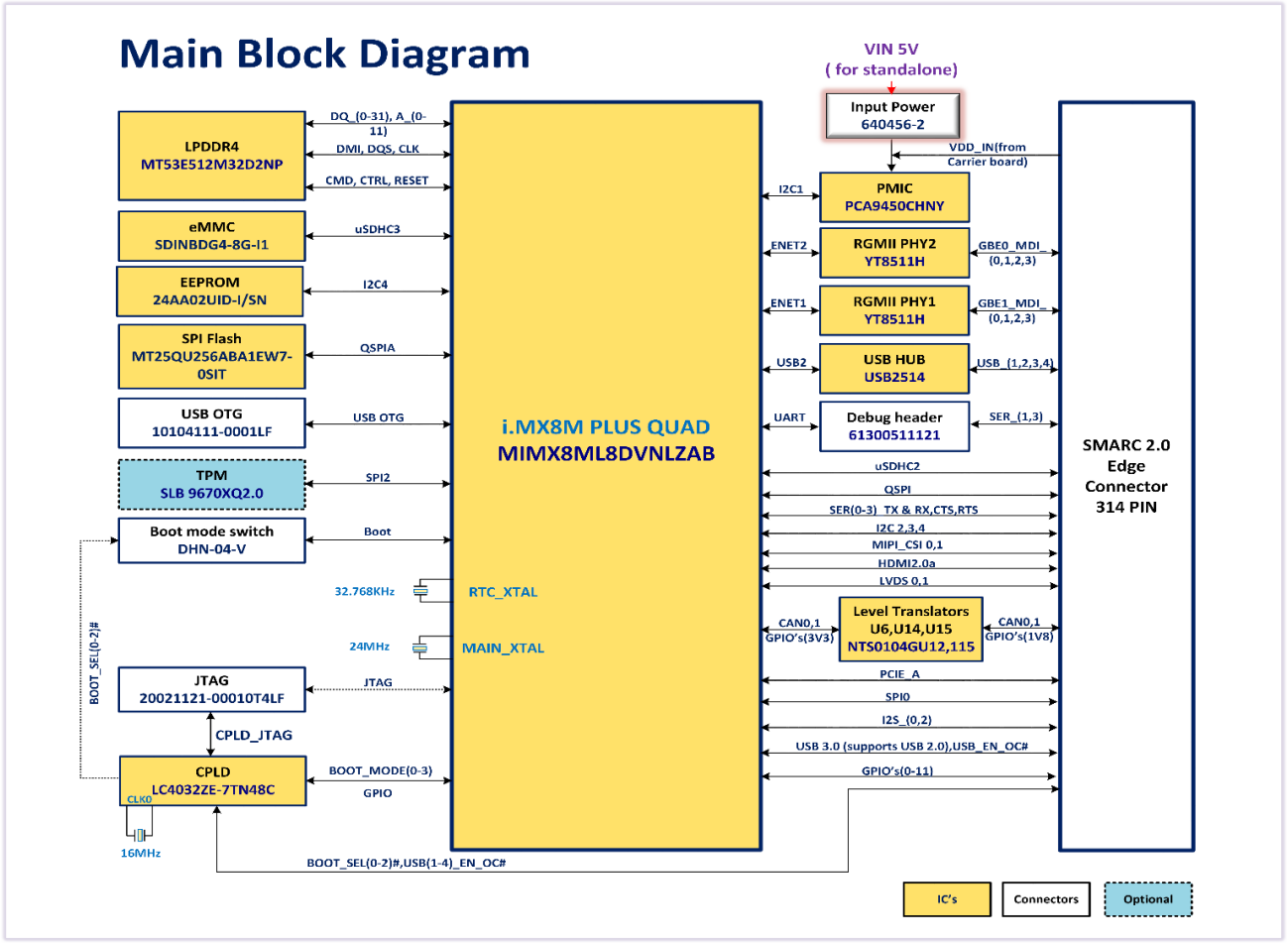

Figure 2 – Module function diagram

4.0. Pinout and Signal Descriptions

The IMX8M Plus SOM Module pins are designated as P1 – P156 on the Module Primary (Top) side, and S1 – S158 on the Module Secondary (Bottom) side. There is a total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used. Some connector vendors offer “reverse” pin-out connectors, which effectively flip the Module over such that the Module Primary side would face the Carrier board.

The SMARC Module pins are deliberately numbered as P1 – P156 and S1 – S158 for clarity and to differentiate the SMARC Module from MXM3 graphics modules, which use the same connector but use the pins for very different functions. MXM3 cards and MXM3 baseboard connectors use a different pin numbering scheme.

The below table is a comprehensible list of all signal pins on the MXM 3 connector in the standard specification SMARC 2.1.

Those signals not supported on IMX8M Plus are strikethroughs.

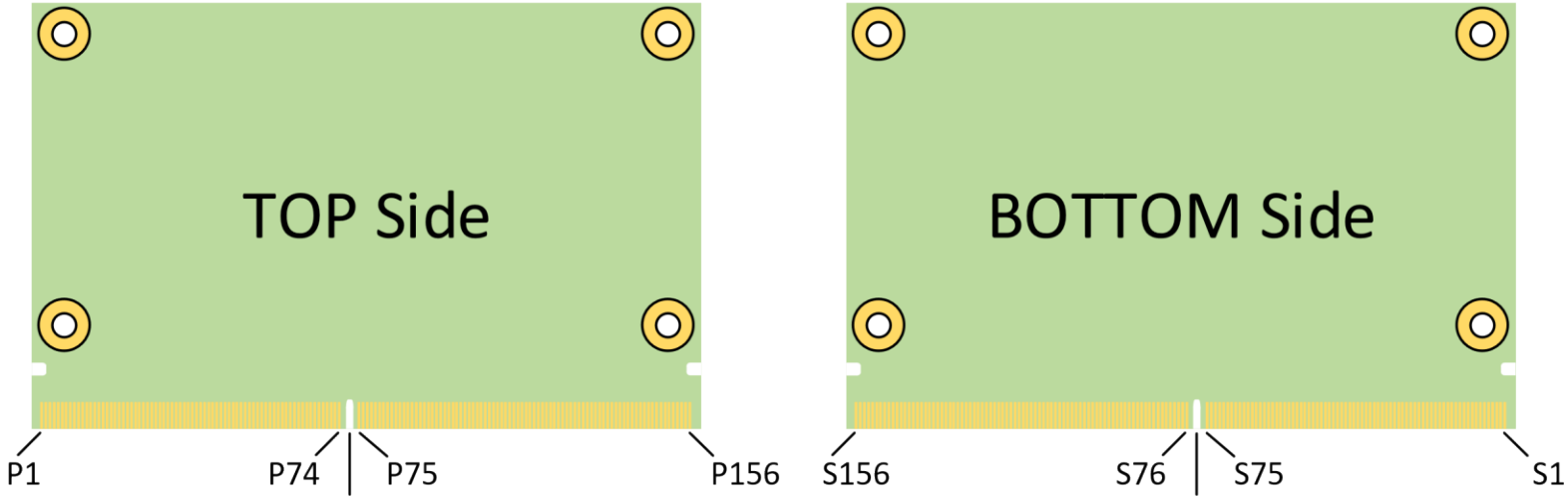

Figure 3 Module top/bottom side pin numbering

4.1. Module Pinout Top Side P

P-Pin Primary (Top) Side	
P1	SMB_ALERT_1V8#
P2	GND
P3	CSI1_CK+
P4	CSI1_CK
P5	GBE1_SDP
P6	GBE0_SDP
P7	CSI1_RX0+
P8	CSI1_RX0-
P9	GND
P10	CSI1_RX1+
P11	CSI1_RX1-
P12	GND
P13	CSI1_RX2+
P14	CSI1_RX2-
P15	GND
P16	CSI1_RX3+
P17	CSI1_RX3-
P18	GND
P19	GBE0_MDI3-

P-Pin Primary (Top) Side	
P21	GBE0_LINK100#
P22	GBE0_LINK1000#
P23	GBE0_MDI2-
P24	GBE0_MDI2+
P25	GBE0_LINK_ACT#
P26	GBE0_MDI1-
P27	GBE0_MDI1+
P28	~~GBE0_CTREF~~
P29	GBE0_MDI0-
P30	GBE0_MDI0+
P31	~~SPI0_CS1#~~
P32	GND
P33	SDIO_WP
P34	SDIO_CMD
P35	SDIO_CD#
P36	SDIO_CK
P37	SDIO_PWR_EN
P38	GND
P39	SDIO_D0

P-Pin Primary (Top) Side	
P41	SDIO_D2
P42	SDIO_D3
P43	SPI0_CS0#
P44	SPI0_CK
P45	SPI0_DIN
P46	SPI0_DO
P47	GND
P48	~~SATA_TX+~~
P49	~~SATA_TX~~
P50	GND
P51	~~SATA_RX+~~
P52	~~SATA_RX~~
P53	GND
P54	ESPI_CS0#
P55	~~ESPI_CS1#~~
P56	ESPI_CK
P57	ESPI_IO_0
P58	ESPI_IO_1
P59	GND

P-Pin Primary (Top) Side	
P61	USB0-
P62	USB0_EN_OC#
P63	USB0_VBUS_DET
P64	USB0_OTG_ID
P65	USB1+
P66	USB1-
P67	USB1_EN_OC#
P68	GND
P69	USB2+
P70	USB2-
P71	USB2_EN_OC#
P72	~~RSVD~~
P73	~~RSVD~~
P74	USB3_EN_OC#
	Key
P75	PCIE_A_RST#
P76	USB4_EN_OC#
P77	~~RSVD~~
P78	~~RSVD~~

P-Pin Primary (Top) Side	
P80	~~PCIE_C_REFCK+~~
P81	~~PCIE_C_REFCK-~~
P82	GND
P83	PCIE_A_REFCK+
P84	PCIE_A_REFCK-
P85	GND
P86	PCIE_A_RX+
P87	PCIE_A_RX-
P88	GND
P89	PCIE_A_TX+
P90	PCIE_A_TX-
P91	GND
P92	HDMI_D2+ / DP1_LANE0+
P93	HDMI_D2- / DP1_LANE0-
P94	GND
P95	HDMI_D1+ / DP1_LANE1+
P96	HDMI_D1- / DP1_LANE1-
P97	GND
P98	HDMI_D0+ / DP1_LANE2+

P20	GBE0_MDI3+

P40	SDIO_D1

P60	USB0+

P79	GND

P99	HDMI_D0- / DP1_LANE2-

P-Pin Primary (Top) Side	
P100	GND
P101	HDMI_CK+ / DP1_LANE3+
P102	HDMI_CK- / DP1_LANE3-
P103	GND
P104	HDMI_HPD / DP1_HPD
P105	HDMI_CTRL_CK / DP1_AUX+
P106	HDMI_CTRL_DAT / DP1_AUX-
P107	~~DP1_AUX_SEL~~
P108	GPIO0 / CAM0_PWR#
P109	GPIO1 / CAM1_PWR#
P110	GPIO2 / CAM0_RST#
P111	GPIO3 / CAM1_RST#

P-Pin Primary (Top) Side	
P112	GPIO4 / HDA_RST#
P113	GPIO5 / PWM_OUT
P114	GPIO6 / TACHIN
P115	GPIO7
P116	GPIO8
P117	GPIO9
P118	GPIO10
P119	GPIO11
P120	GND
P121	I2C_PM_CK
P122	I2C_PM_DAT
P123	BOOT_SEL0#
P124	BOOT_SEL1#
P125	BOOT_SEL2#
P126	RESET_OUT#

P-Pin Primary (Top) Side	
P127	RESET_IN#
P128	POWER_BTN#
P129	SER0_TX
P130	SER0_RX
P131	SER0_RTS#
P132	SER0_CTS#
P133	GND
P134	SER1_TX
P135	SER1_RX
P136	SER2_TX
P137	SER2_RX
P138	SER2_RTS#
P139	SER2_CTS#
P140	SER3_TX
P141	SER3_RX

P-Pin Primary (Top) Side	
P142	GND
P143	CAN0_TX
P144	CAN0_RX
P145	CAN1_TX
P146	CAN1_RX
P147	VDD_IN
P148	VDD_IN
P149	VDD_IN
P150	VDD_IN
P151	VDD_IN
P152	VDD_IN
P153	VDD_IN
P154	VDD_IN
P155	VDD_IN
P156	VDD_IN

4.2. Module Pinout Bottom Side S

SPin Secondary (Bott) Side	
S1	CSI1_TX+ / I2C_CAM1_CK
S2	CSI1_TX- / I2C_CAM1_DAT
S3	GND
S4	~~RSVD~~
S5	~~CSI0_TX- / I2C_CAM0_CK~~
S6	CAM_MCK
S7	~~CSI0_TX+ / I2C_CAM0_DAT~~
S8	CSI0_CK+
S9	CSI0_CK-
S10	GND
S11	CSI0_RX0+
S12	CSI0_RX0-
S13	GND
S14	CSI0_RX1+
S15	CSI0_RX1-
S16	GND
S17	GBE1_MDI0+
S18	GBE1_MDI0-
S19	GBE1_LINK100#
S20	GBE1_MDI1+

SPin Secondary (Bott) Side	
S21	GBE1_MDI1-
S22	GBE1_LINK1000#
S23	GBE1_MDI2+
S24	GBE1_MDI2-
S25	GND
S26	GBE1_MDI3+
S27	GBE1_MDI3-
S28	~~GBE1_CTREF~~
S29	PCIE_D_TX+
S30	PCIE_D_TX-
S31	GBE1_LINK_ACT#
S32	PCIE_D_RX+
S33	PCIE_D_RX-
S34	GND
S35	USB4+
S36	USB4-
S37	~~USB3_VBUS_DET~~
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT

SPin Secondary (Bott) Side	
S41	I2S0_SDIN
S42	I2S0_CK
S43	ESPI_ALERT0#
S44	ESPI_ALERT1#
S45	~~RSVD~~
S46	~~RSVD~~
S47	GND
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	HDA_SYNC / I2S2_LRCK
S51	HDA_SDO / I2S2_SDOUT
S52	HDA_SDI / I2S2_SDIN
S53	HDA_CK / I2S2_CK
S54	~~SATA_ACT#~~
S55	~~USB5_EN_OC#~~
S56	ESPI_IO_2
S57	ESPI_IO_3
S58	ESPI_RESET#
S59	~~USB5+~~
S60	~~USB5-~~

SPin Secondary (Bott) Side	
S61	GND
S62	USB3_SSTX+
S63	USB3_SSTX-
S64	GND
S65	USB3_SSRX+
S66	USB3_SSRX-
S67	GND
S68	USB3+
S69	USB3-
S70	GND
S71	USB2_SSTX+
S72	USB2_SSTX-
S73	GND
S74	USB2_SSRX+
S75	USB2_SSRX-
	KEY
S76	~~PCIE_B_RST#~~
S77	~~PCIE_C_RST#~~
S78	~~PCIE_C_RX+~~
S79	~~PCIE_C_RX-~~

SPin Secondary (Bott) Side	
S80	GND
S81	~~PCIE_C_TX+~~
S82	~~PCIE_C_TX-~~
S83	GND
S84	~~PCIE_B_REFCK+~~
S85	~~PCIE_B_REFCK-~~
S86	GND
S87	~~PCIE_B_RX+~~
S88	~~PCIE_B_RX-~~
S89	GND
S90	~~PCIE_B_TX+~~
S91	~~PCIE_B_TX-~~
S92	GND
S93	DP0_LANE0+
S94	DP0_LANE0-
S95	DP0_AUX_SEL
S96	~~DP0_LANE1+~~
S97	~~DP0_LANE1-~~
S98	DP0_HPD
S99	~~DP0_LANE2+~~

SPin Secondary (Bott) Side	
S100	~~DP0_LANE2-~~
S101	GND
S102	~~DP0_LANE3+~~
S103	~~DP0_LANE3-~~
S104	~~USB3_OTG_ID~~
S105	~~DP0_AUX+~~
S106	~~DP0_AUX-~~
S107	LCD1_BKLT_EN
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-
S110	GND
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-
S113	~~eDP1_HPD~~
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+

SPin Secondary (Bott) Side	
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-
S116	LCD1_VDD_EN
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-
S119	GND
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-
S122	LCD1_BKLT_PWM
S123	~~RSVD~~
S124	GND
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-
S127	LCD0_BKLT_EN
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-

SPin Secondary (Bott) Side	
S130	GND
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-
S133	LCD0_VDD_EN
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-
S136	GND
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-
S139	I2C_LCD_CK
S140	I2C_LCD_DAT
S141	LCD0_BKLT_PWM
S142	~~RSVD~~
S143	GND
S144	~~eDP0_HPD~~

SPin Secondary (Bott) Side	
S145	~~WDT_TIME_OUT#~~
S146	PCIE_WAKE#
S147	~~VDD_RTC~~
S148	LID#
S149	SLEEP#
S150	VIN_PWR_BAD#
S151	CHARGING#
S152	CHARGER_PRSNT#
S153	CARRIER_STBY#
S154	CARRIER_PWR_ON
S155	FORCE_RECOV#
S156	BATLOW#
S157	TEST#
S158	GND

4.3 Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with mandatory PU (pull up) on module
OD	Open drain
I/O	Bi-directional Input/Output
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module
VDD_IN	Main power source from carrier to module
CMOS	Logic input or output
GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	Low Voltage Differential Signal for DisplayPort interface
LVDS D-PHY	Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays
LVDS M-PHY	Low Voltage Differential Signal for MIPI CSI-3 cameras
LVDS LCD	Low Voltage Differential Signal for LCD displays
LVDS PCIE	Low Voltage Differential Signal for PCIe
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
3.3V	3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)

4.3.1 LVDS0/LVDS1 MODE

IMX8M Plus has integrated the Dual channel LVDS0 & LVDS1. The following table shows the pins of the SMARC connector are used when the LVDS feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
D29 E28 E29 F28 G29 H28 H29 J28	**LVDS0_0+** **LVDS0_0-** **LVDS0_1+** **LVDS0_1-** **LVDS0_2+** **LVDS0_2-** **LVDS0_3+** **LVDS0_3-**	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
F29 G28	**LVDS0_CK+** **LVDS0_CK-**	S134 S135	Primary LVDS channel differential pair clock lines	O LVDS LCD		Runtime		
W25	**LCD0_VDD_EN**	S133	Primary LVDS channel power enable, active high	O CMOS	1.8V	Runtime		
Y29	**LCD0_BKLT_EN**	S127	Primary LVDS channel backlight enable, active high	O CMOS	1.8V	Runtime		
AE18	**LCD0_BKLT_PWM**	S141	Primary LVDS channel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
A26 B26 A27 B27 B29 C28 C29 D28	**LVDS1_0+** **LVDS1_0-** **LVDS1_1+** **LVDS1_1-** **LVDS1_2+** **LVDS1_2-** **LVDS1_3+** **LVDS1_3-**	S111 S112 S114 S115 S117 S118 S120 S121	Secondary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
A28 B28	**LVDS1_CK+** **LVDS1_CK-**	S108 S109	Secondary LVDS channel differential pair clock lines.	O LVDS LCD		Runtime		
W26	**LCD1_VDD_EN**	S116	Secondary panel power enable, active high	O CMOS	1.8V	Runtime		
Y28	**LCD1_BKLT_EN**	S107	Secondary panel backlight enable, active high	O CMOS	1.8V	Runtime		
AC18	**LCD1_BKLT_PWM**	S122	Secondary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
AJ6	**I2C_LCD_DAT**	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
AJ7	**I2C_LCD_CK**	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.3.2 MIPI CSI1 (Camera)

IMX8M Plus has integrated a MIPI-CSI interface with up-to four data lanes and one clock lanes with MIPI D-PHY specification V1.2 The following table shows the pins of the SMARC connector are used when the MIPI CSI feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
D18 E18 D20 E20 D24 E24 D26 E26	**CSI1_RX0+** **CSI1_RX0-** **CSI1_RX1+** **CSI1_RX1-** **CSI1_RX2+** **CSI1_RX2-** **CSI1_RX3+** **CSI1_RX3-**	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY		Runtime		
D22 E22	**CSI1_CK+** **CSI1_CK-**	P3 P4	CSI1 differential clock input (point to point)	I LVDS D-PHY		Runtime		
AE8	**I2C_CAM1_DAT /** ~~**CSI1_TX-**~~	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS MPHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_DAT MIPI-CSI 3.0 mode uses CSI1_TX-
AH6	**I2C_CAM1_CK /** ~~**CSI1_TX+**~~	S1	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_CK MIPI-CSI 3.0 mode uses CSI1_TX+
AA29	**CAM1_PWR# / GPIO1**	P109	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO1 can be enabled through DVT
A7	**CAM1_RST# / GPIO3**	P111	Camera 0 reset, active low output	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO3 can be enabled through DVT
K29	**CAM_MCK**	S6	Master clock output	O CMOS	1.8V	Runtime		This signal is used by both CSI0 and CSI1

A25 B25 A24 B24	**CSI0_RX0+** **CSI0_RX0-** **CSI0_RX1+** **CSI0_RX1-**	S11 S12 S14 S15	CSI0 differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY		Runtime		

A23 B23 A22 B22 A21 B21	**CSI0_CK+** **CSI0_CK-** **CSI0_D2+** **CSI0_D2-** **CSI0_D3+** **CSI0_D3-**	S8 S9 S32 S33 S29 S30	CSI0 differential clock input (point to point)	I LVDS D-PHY		Runtime		**CSI0_D2+** **CSI0_D2-** **CSI0_D3+** **CSI0_D3-** Signals are connected to PCIe TX, RX pin,

4.3.3 I2S (Audio)

IMX8M Plus has integrated a I2S interface The I2S (or I2S) module provides a synchronous audio interface (SAI) that supports, full-duplex serial interfaces with frame synchronization.
The following table shows the pins of the SMARC connector that are used when the I2S feature is enabled.

Ball#	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AC16	**I2S0_LRCK**	S39	I2S0 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AH18	**I2S0_SDOUT**	S40	I2S0 Digital audio Output	O CMOS	1.8V	Runtime		
AF18	**I2S0_SDIN**	S41	I2S0 Digital audio Input	I CMOS	1.8V	Runtime		
AH19	**I2S0_CK**	S42	I2S0 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AJ17	**I2S2_LRCK**	S50	I2S2 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AH16	**I2S2_SDOUT**	S51	I2S2 Digital audio Output	O CMOS	1.8V	Runtime		
AJ14	**I2S2_SDIN**	S52	I2S2 Digital audio Input	I CMOS	1.8V	Runtime		
AH15	**I2S2_CK**	S53	I2S2 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AJ20	**AUDIO_MCK**	S38	Master clock output to I2S co-dec(s)	O CMOS	1.8V	Runtime		

4.3.4 USB 3.0 Ports

IMX8M Plus has integrated a USB Hub 3 and 2.0.

The following table shows the pins of the SMARC connector are used when the USB HUB feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
	USB0+ **USB0-**	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Runtime		**Connected to USB HUB**
B5	**USB0_EN_OC#**	P62	USB over-current sense for port 0	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
A11	**USB0_VBUS_DET**	P63	USB port 0 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Runtime		Can be connected to a USB client port VBUS pin
B11	**USB0_OTG_ID**	P64	Input pin to announce OTG device insertion on USB 2.0 port	I CMOS	3.3Vsb / 3.3V	Runtime		
	USB1+ **USB1-**	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Runtime		**Connected to USB HUB**.
	USB1_EN_OC#	P67	USB over-current sense for port 1	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	**Connected to CPLD.** Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
	USB2+ **USB2-**	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Runtime		**Connected to USB HUB**

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
A9 B9	**USB2_SSRX+** **USB2_SSRX-**	S74 S75	Receive signal differential pairs for SuperSpeed on port 2	I USB SS	USB SS	Runtime		
A10 B10	**USB2_SSTX+** **USB2_SSTX-**	S71 S72	Transmit signal differential pairs for SuperSpeed on port 2	O USB SS	USB SS	Runtime		
	USB2_EN_OC#	P71	USB over-current sense for port 2	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	**Connected to CPLD** Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
	USB3+ **USB3-**	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Runtime		**Connected to USB HUB**
A12 B12	**USB3_SSRX+** **USB3_SSRX-**	S65 S66	Receive signal differential pairs for SuperSpeed on port 3	I USB SS	USB SS	Runtime		
A13 B13	**USB3_SSTX+** **USB3_SSTX-**	S62 S63	Transmit signal differential pairs for SuperSpeed on port 3	O USB SS	USB SS	Runtime		
	USB3_EN_OC#	P74	USB over-current sense for port 3	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	**Connected to CPLD** Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
	~~**USB3_VBUS_DET**~~	~~S37~~	~~USB port 3 host power detection, when this port is used as a device~~.	I ~~USB VBUS 5V~~	~~USB VBUS 5V~~	~~Runtime~~		

	~~**USB3_OTG_ID**~~	~~S104~~	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I CMOS~~	~~3.3Vsb / 3.3V~~	~~Runtime~~		

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
	USB4+ **USB4-**	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Runtime		**Connected to USB HUB**
	USB4_EN_OC#	P76	USB over-current sense for port 4	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	**Connected to CPLD.** Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
	~~**USB5+**~~ ~~**USB5-**~~	~~S59~~ ~~S60~~	~~USB differential data pairs for port 5~~	~~I/O USB~~	~~USB~~	~~Standby~~		
	~~**USB5_EN_OC#**~~	~~S55~~	~~USB over-current sense for port 5~~	~~I/O OD CMOS~~	~~3.3Vsb / 3.3V~~	~~Standby~~	~~PU 10k~~	~~Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation~~.

4.3.5 PCIe Port

IMX8M Plus the module supports one PCIe Gen 2.1 ports (PCIE_A).

The following table shows the pins of the SMARC connector are used when the PCIe feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
A15 B15	**PCIE_A_TX+** **PCIE_A_TX-**	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
A14 B14	**PCIE_A_RX+** **PCIE_A_RX-**	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
D16 E16	**PCIE_A_REFCK+** **PCIE_A_REFCK-**	P83 P84	Differential PCIe Link A reference clock output	O LVDS PCIE		Runtime		
AE16	**PCIE_A_RST#**	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		Connected through Level Translator
AD14	**PCIE_WAKE#**	S146	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	I OD CMOS	3.3V	Runtime	PU 10k	Connected through Level Translator
A21 B21	**PCIE_D_TX+** **PCIE_D_TX-**	S29 S30	Differential PCIe link D transmit data pair OR CSI0 differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY,PCIE		Runtime		this pin used for CSI0_D3_P & CSI0_D3_N and added 0-ohm resistors R299 & R300(made it DNP)
A22 B22	**PCIE_D_RX+** **PCIE_D_RX-**	S32 S33	Differential PCIe link A receive data pair OR CSI0 differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY,PCIE		Runtime		this pin used for CSI0_D2_P & CSI0_D2_N and added 0-ohm resistors R299 & R300(made it DNP)

4.3.6 HDMI Port

IMX8M Plus the module supports one HDMI 2.0a ports (HDMI).
The following table shows the pins of the SMARC connector are used when the HDMI feature is enabled

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AH25 AJ25	**HDMI_D0+** **HDMI_D0-**	P98 P99	HDMI Port, Differential Pair Data Lines	O TMDS HDMI		Runtime		
AH26 AJ26	**HDMI_D1+** **HDMI_D1-**	P95 P96	HDMI Port, Differential Pair Data Lines	O TMDS HDMI		Runtime		
AH27 AJ27	**HDMI_D2+** **HDMI_D2-**	P92 P93	HDMI Port, Differential Pair Data Lines	O TMDS HDMI		Runtime		
AH24 AJ24	**HDMI_CK+** **HDMI_CK-**	P101 P102	HDMI Port, Differential Pair Clock Lines	O TMDS HDMI		Runtime		
AC22	**HDMI_CTRL_CK**	P105	I2C_CLK Line Dedicated to HDMI	I/O OD CMOS	1.8V	Runtime	PU 100k	
AF22	**HDMI_CTRL_DAT**	P106	I2C_DAT Line Dedicated to HDMI	I/O OD CMOS	1.8V	Runtime	PU 100k	
AE22	**HDMI_HPD**	P104	HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	I CMOS	1.8V	Runtime	PU 100k	

4.3.7 LAN Port

IMX8M Plus the module supports two LAN ports is derived from the SOCs RGMII interface.
The following table shows the pins of the SMARC connector that are used when the Ethernet feature is enabled.

Ethernet1:

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
--- --- --- --- --- --- --- --- ---	**GBE0_MDI0+** **GBE0_MDI0-** **GBE0_MDI1+** **GBE0_MDI1-** **GBE0_MDI2+** **GBE0_MDI2-** **GBE0_MDI3+** **GBE0_MDI3-**	P30 P29 P27 P26 P24 P23 P20 P19	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	GBE MDI		Runtime		**Connected to ETH-PHY.** Twisted pair signals for external transformer.
---	**GBE0_LINK100#**	P21	Link Speed Indication LED for GBE 0 100Mbps	O OD CMOS	3.3V	Runtime		**Connected to ETH-PHY.** Shall be able to sink 24mA or more Carrier LED current
----	**GBE0_LINK1000#**	P22	Link Speed Indication LED for GBE 0 1000Mbps	O OD CMOS	3.3V	Runtime		**Connected to ETH-PHY.** Shall be able to sink 24mA or more Carrier LED current

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
-----	**GBE0_LINK_ACT#**	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 Mbps) Blinks on Activity	O OD CMOS	3.3V	Runtime		**Connected to ETH-PHY.** Shall be able to sink 24mA or more Carrier LED current
	~~**GBE0_CTREF**~~	~~P28~~	~~Center Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~	~~Analog~~	~~0 to 3.3V max~~	~~Runtime~~		
-----	**GBE0_SDP**	P6	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)	IO CMOS	3.3V	Runtime		Connected to Test point.

Ethernet2:

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
- - - - - - - - -	**GBE1_MDI0+** **GBE1_MDI0-** **GBE1_MDI1+** **GBE1_MDI1-** **GBE1_MDI2+** **GBE1_MDI2-** **GBE1_MDI3+** **GBE1_MDI3-**	S17 S18 S20 S21 S23 S24 S26 S27	Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	GBE MDI		Runtime		**Connected to ETH-PHY.** Twisted pair signals for external transformer.
---	**GBE1_LINK100#**	S19	Link Speed Indication LED for GBE 1 100Mbps	O OD CMOS	3.3V	Runtime		**Connected to ETH-PHY.** Shall be able to sink 24mA or more Carrier LED current
----	**GBE1_LINK1000#**	S22	Link Speed Indication LED for GBE 1 1000Mbps	O OD CMOS	3.3V	Runtime		**Connected to ETH-PHY.** Shall be able to sink 24mA or more Carrier LED current

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
----	**GBE1_LINK_ACT#**	S31	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 Mbps) Blinks on Activity	O OD CMOS	3.3V	Runtime		**Connected to ETH-PHY.** Shall be able to sink 24mA or more Carrier LED current
	~~**GBE1_CTREF**~~	~~S28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~	~~Analog~~	~~0 to 3.3V max~~	~~Runtime~~		
-----	**GBE1_SDP**	P5	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)	IO CMOS	3.3V	Runtime		Connected to Test point.

4.3.8 SDIO Port

IMX8M Plus the module supports one MMC/SD/SDIO port. The port is derived from the i.MX8M Plus on-chip MMC/SD/SDIO controller (uSDHC2). The following table shows the pins of the SMARC connector are used when the SDIO feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AC28 AC29 AA26 AA25	**SDIO_D0** **SDIO_D1** **SDIO_D2** **SDIO_D3**	P39 P40 P41 P42	SDIO Data lines. These signals operate in push- pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
AC26	**SDIO_WP**	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
AB28	**SDIO_CMD**	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
AD29	**SDIO_CD#**	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
AB29	**SDIO_CK**	P36	SDIO Clock. With each cycle of this signal a one- bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		

---	**SDIO_PWR_EN**	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device on the Carrier board.	O CMOS	3.3V	Runtime		Connected the SDIO_PWR_EN signal to the NVCC_SD2 for supplying the uSD in carrier board.

4.3.9 SPI0 Port

IMX8M Plus the module supports one SPI port. Full duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes.

The following table shows the pins of the SMARC connector that are used when the SPI0 feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AJ22	**SPI0_CS0#**	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
	~~**SPI0_CS1#**~~	~~P31~~	~~SPI0 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	~~Standby~~		
AH21	**SPI0_CK**	P44	SPI0 Clock	O CMOS	1.8V	Standby		
AH20	**SPI0_DIN**	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
AJ21	**SPI0_DO**	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

4.3.10 QSPI (ECSPI) Port

IMX8M Plus the module supports one Quad SPI serial flash device, each with up to four bidirectional data lines.

loopback mode).

The following table shows the pins of the SMARC connector are used when the QSPI feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
L26	**ESPI_CS0#**	P54	ESPI1 Master Chip Select 0	O CMOS	1.8V	Standby		
	~~**ESPI_CS1#**~~	~~P55~~	~~ESPI1 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	~~Standby~~		
N25	**ESPI_CK**	P56	ESPI Master Clock output	O CMOS	1.8V	Standby		
A4	**ESPI_RESET#**	S58	ESPI Reset	O CMOS	1.8V	Standby		Reset the ESPI interface for both master and slaves. ESPI Reset# is typically driven from ESPI master to ESPI slaves
V28 A6	**ESPI_ALERT0#** **ESPI_ALERT1#**	S43 S44	ESPI ALERT	I OD CMOS	1.8V	Standby		This pin is used by ESPI slave to request service from ESPI. master. Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.
L25 R25 L24 N24	**ESPI_IO_1** **ESPI_IO_0** **ESPI_IO_2** **ESPI_IO_3**	P58 P57 S56 S57	ESPI Master Data Input / Out-put.	I/O CMOS	1.8V	Standby		ESPI_IO_0 can also be used as SPI1_DO (MOSI) ESPI_IO_1 can also be used as SPI1_DIN (MISO) In Single I/O mode, ESPI_IO_0 is the ESPI master output / ESPI slave input (MOSI) whereas

								ESPI_IO_1 is the SPI master input / ESPI slave output (MISO).

4.3.11 General purpose I2C

The SMARC specification supports a total of 6 different I2C busses on its pinout. Most of these busses are designated for specific functions such as I2C for camera management, LVDS panels or I2C for PMIC. Just one I2C bus is marked as General purpose.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AD8	**I2C_GP_DAT**	S49	General purpose I2C data signal	I/O OD CMOS	1.8V	Runtime	PU 2k2	Connected to EEPROM I2C SDA signal
AF8	**I2C_GP_CK**	S48	General purpose I2C clock signal	O OD CMOS	1.8V	Runtime	PU 2k2	Connected to EEPROM I2C SCL signal

Most of the other I2C buses are described in their designated function tables rather than in a single big list.

Below is an overview of all I2C busses and where to find them.

Ball#	Name	Pin #	Description	Where to find
AJ6	I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	LVDS / DSI / eDP tables
AJ7	I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	LVDS / DSI / eDP tables
AE8	I2C_CAM1_DAT	S2	I2C data for serial camera data support link	MIPI CSI table
AH6	I2C_CAM1_CK	S1	I2C clock for serial camera data support link	MIPI CSI table
AH7	I2C_PM_DAT	P122	Power management I2C bus DATA (SMBus for x86)	Power and System Management
AC8	I2C_PM_CK	P121	Power management I2C bus CLK (SMBus for x86)	Power and System Management

4.3.12 General purpose I/O (GPIO)

IMX8M Plus the module supports one 12 GPIO lines that are required by the SMARC 2.0 standard.

The following table shows the pins of the SMARC connector are used when the GPIO feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
U26	**GPIO0**	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470K on the Module.	Default use is GPIO0
AA29	**GPIO1**	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO1
AA28	**GPIO2**	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO2
A7	**GPIO3**	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO3
E8	**GPIO4**	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
E6	**GPIO5**	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
B4	**GPIO6**	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
A3	**GPIO7**	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
F6	**GPIO8**	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
A8	**GPIO9**	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
B8	**GPIO10**	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	

A5	**GPIO11**	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	

4.3.13 UART

IMX8M Plus the module supports 4 universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The following table shows the pins of the SMARC connector are used when the UART feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AJ3	SER0_TX	P129	Asynchronous serial data output port 0	O CMOS	1.8V	Runtime		
AD6	SER0_RX	P130	Asynchronous serial data input port 0	I CMOS	1.8V	Runtime		
AJ4	SER0_RTS#	P131	"Request to Send" handshake line for port 0	O CMOS	1.8V	Runtime		
AE6	SER0_CTS#	P132	"Clear to Send" handshake line for port 0	I CMOS	1.8V	Runtime		
AH4	SER1_TX	P134	Asynchronous serial data output port 1	O CMOS	1.8V	Runtime		
AF6	SER1_RX	P135	Asynchronous serial data input port 1	I CMOS	1.8V	Runtime		
AC20	SER2_TX	P136	Asynchronous serial data output port 2	O CMOS	1.8V	Runtime		
AF20	SER2_RX	P137	Asynchronous serial data input port 2	I CMOS	1.8V	Runtime		
AE20	SER2_RTS#	P138	"Request to Send" handshake line for port 2	O CMOS	1.8V	Runtime		
AD20	SER2_CTS#	P139	"Clear to Send" handshake line for port 2	I CMOS	1.8V	Runtime		
AH5	SER3_TX	P140	Asynchronous serial data output port 3	O CMOS	1.8V	Runtime		
AJ5	SER3_RX	P141	Asynchronous serial data input port 3	I CMOS	1.8V	Runtime		

4.3.14 CAN BUS

IMX8M Plus the module supports 2 CAN V2.0B at 1 Mb/s.

The following table shows the pins of the SMARC connector that are used when the CAN feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AD16	CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	3.3V	Runtime		Connected through Level Translator
AF16	CAN0_RX	P144	CAN port 0 Receive input	I CMOS	3.3V	Runtime		Connected through Level Translator
AE14	CAN1_TX	P145	CAN port 1 Transmit output	O CMOS	3.3V	Runtime		Connected through Level Translator
AF14	CAN1_RX	P146	CAN port1 Receive input	I CMOS	3.3V	Runtime		Connected through Level Translator

4.3.15 Miscellaneous

The following table shows the pins of the SMARC connector are used when the Miscellaneous feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
AD18	**TEST#**	S157	Held low by Carrier to invoke Module vendor specific test function(s).	I CMOS	1.8V	Runtime	PU on Mod- ule. Driven by OD on Carrier	A module must implement PU but actual value is dependent on particular module design. Carrier Board should leave this pin floating for normal operation

4.3.16 Power and System Management

The following table shows the pins of the SMARC connector are used when the Power and System Management feature is enabled.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
B7	BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module
AJ13	CARRIER_PWR_ON	S154	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8Vsb / 1.8V	-		1.8Vsb is only used for signaling, not a power source to the module Connected through Level Translator
AC12	CARRIER_STBY#	S153	The Module shall drive this signal low when the system is in a standby power state.	O CMOS	1.8Vsb / 1.8V	-		Connected through Level Translator
AJ15	CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
D8	CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
---	VIN_PWR_BAD#	S150	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.	I OD CMOS	1.8V	Runtime	PU 2.2K	**Connected to CPLD** Driven by OD on Carrier Module must implement PU but actual value is depended on particular mod- ule design.
AE12	SLEEP#	S149	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module. Connected through Level Translator

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
---	LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	**Connected to CPLD.** Driven by OD on Carrier. Pulled up on module.
G22	POWER_BTN#	P128	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
AJ19	RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	1.8V	Runtime		
---	RESET_IN#	P127	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	1.8V	Runtime	PU 4.7K	**Connected to PMIC.** Driven by OD on Carrier. Pulled up on module.
AH7	I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB DATA. Pulled up on module.
AC8	I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB CLK. Pulled up on module.
---	SMB_ALERT_1V8#	P1	SMBus Alert# (interrupt) signal	I OD CMOS	1.8V	Runtime	PU 2k2	Connected to CPLD. only used on x86 design

4.3.17 Boot Select

The following table shows the pins of the SMARC connector are used when the Boot selection.

Ball #	Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
-- -	**BOOT_SEL0#** **BOOT_SEL1#** **BOOT_SEL2#**	P123 P124 P125	Input straps determine the Module boot	I OD CMOS	1.8Vsb	Standby	PU 4.7K	. **Connected to CPLD.** Driven by OD on Carrier. Pulled up on module. Booting from eMMC and SD card is supported
W28	**FORCE_RECOV#**	S155		I OD CMOS	1.8Vsb	Standby	PU 10K	. Driven by OD on Carrier. Pulled up on module.

4.3.18 Power

The following table shows the pins of the SMARC connector are used for the power supply of the board.

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	3 to 5.25V / 5V		Connected to input Power connector.
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	Ground		Connected to Ground

4.4. Module Outline – 82mm x 50mm Module

The Figure 2 on the following page details the 82mm x 50mm IMX8M Plus SOM mechanical attributes, including the pin numbering and edge finger pattern.

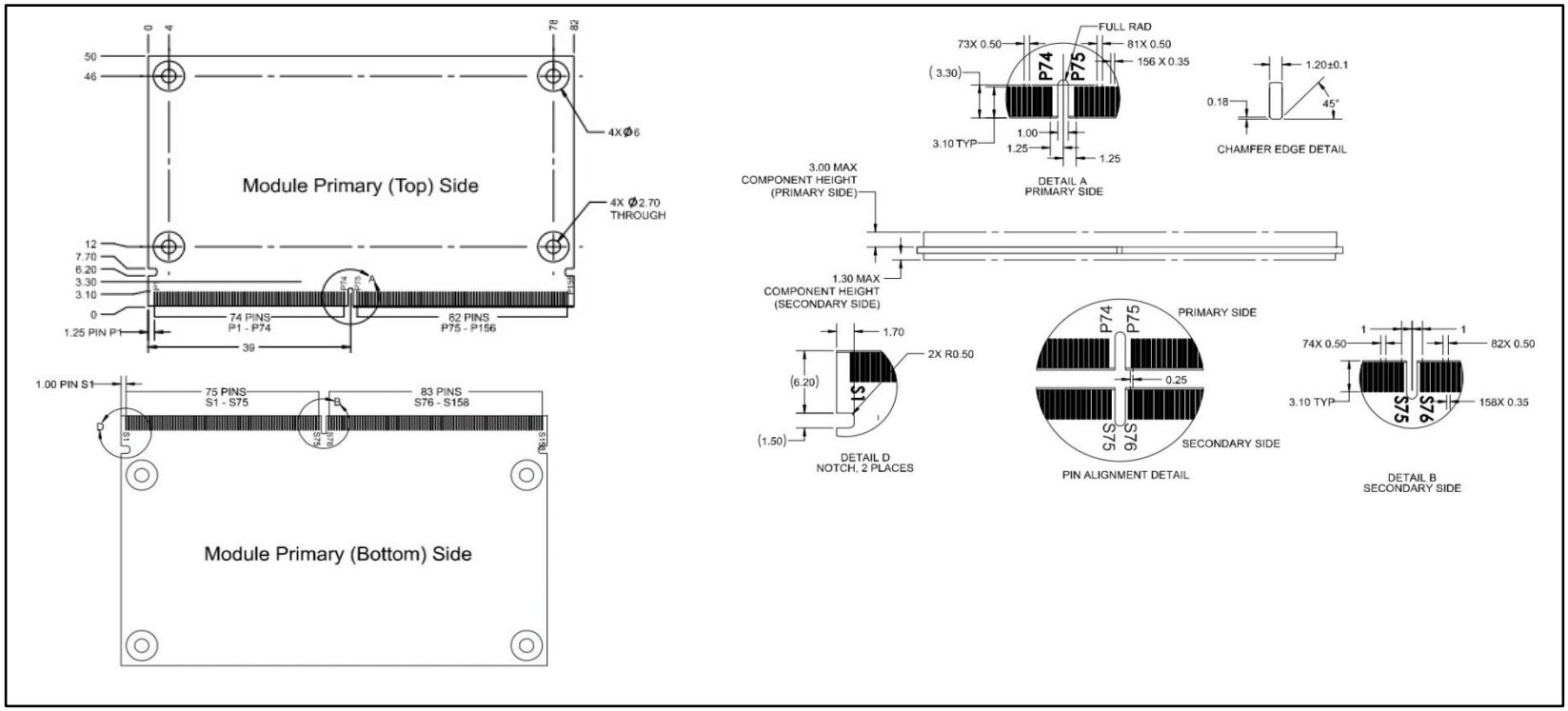

Figure 4 Module Outline

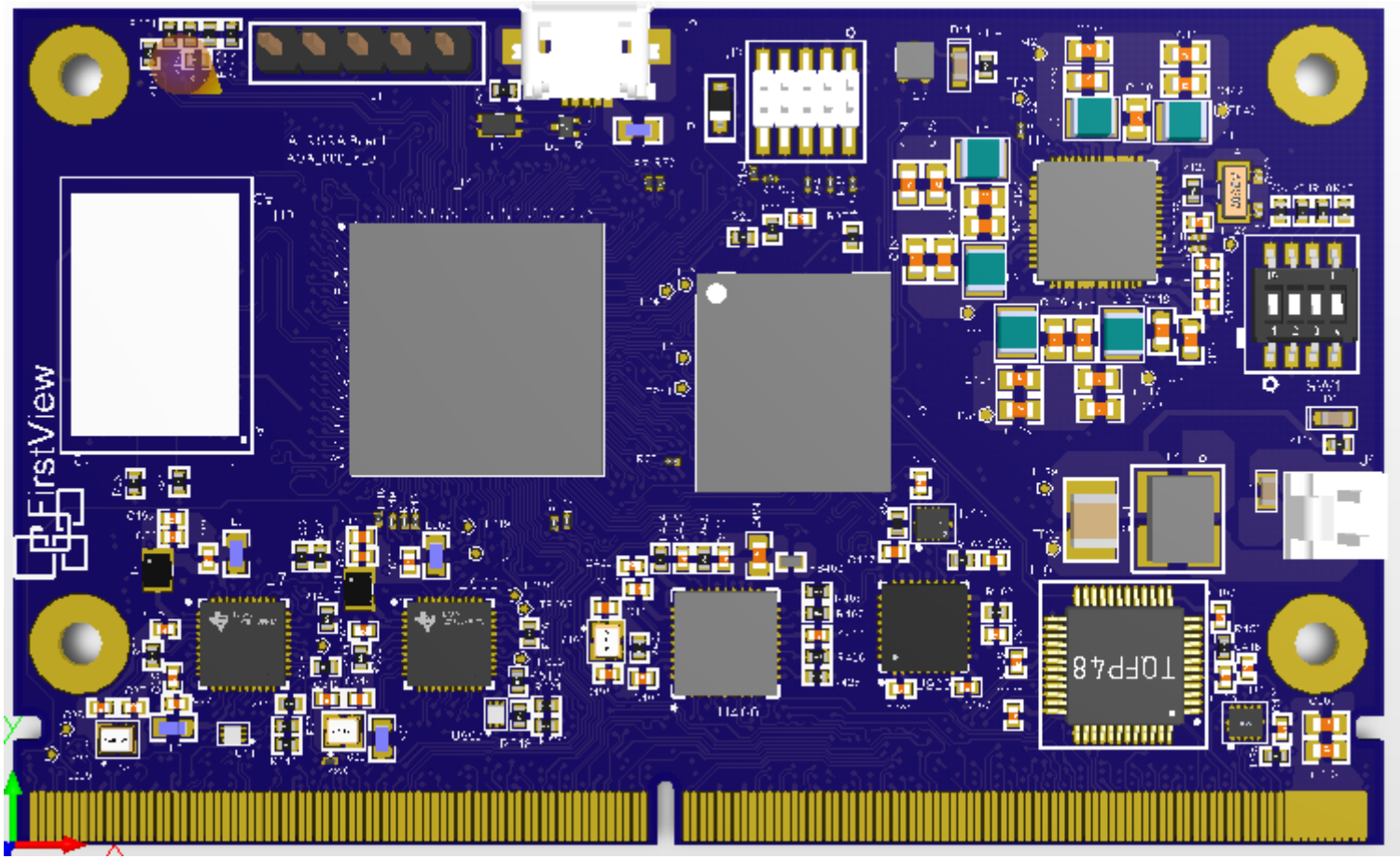

Figure 5 Module Top View (3D)

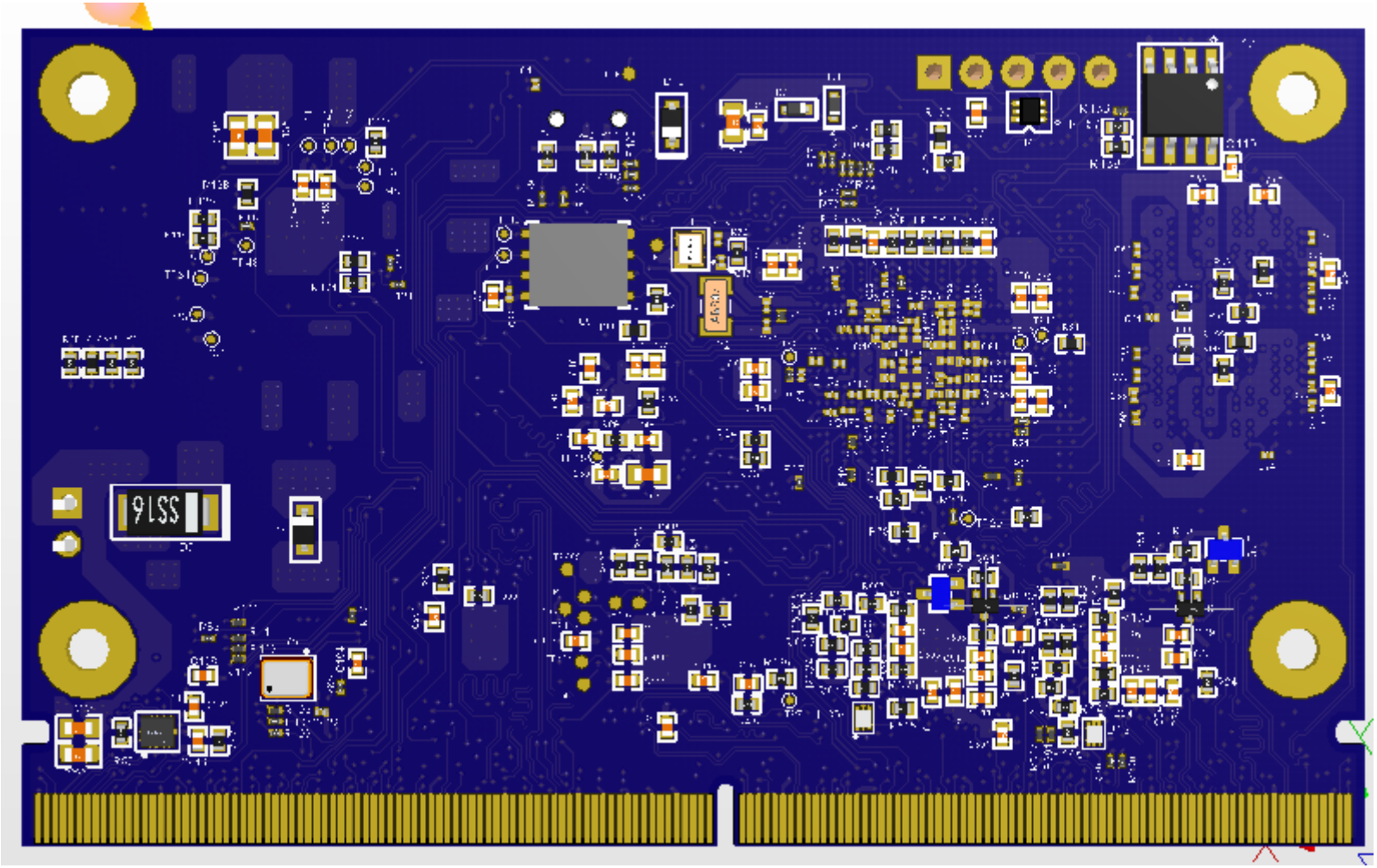

Figure 6 Module Bottom View (3D)

Technical Support

MAS Elettronica provides its product with one-year free technical support including:

1. Providing software and hardware resources related to the embedded products of MAS Elettronica;
2. Helping customers properly compile and run the source code provided by MAS Elettronica;
3. Providing technical support service if the embedded hardware products do not function properly under the circumstance that customers operate according to the instructions in the documents provided by MAS Elettronica;
4. Helping customers troubleshoot the products.

The following conditions will not be covered by our technical support service. We will take appropriate measures accordingly:

a. Customers encounter issues related to software or hardware during their development process;
b. Customers encounter issues caused by any unauthorized alter to the embedded operating system;
c. Customers encounter issues related to their own applications;
d. Customers encounter issues caused by any unauthorized alter to the source code provided by MAS Elettronica;

Warranty Conditions

- 12-month free warranty on the PCB under normal conditions of use since the sales of the product;
- The following conditions are not covered by free services; MAS Elettronica will charge accordingly:

Customers fail to provide valid purchase vouchers or the product identification tag is damaged, unreadable, altered or inconsistent with the products.
Products are damaged caused by operations inconsistent with the user manual;
Products are damaged in appearance or function caused by natural disasters (flood, fire, earthquake, lightning strike or typhoon) or natural aging of components or other force majeure;
Products are damaged in appearance or function caused by power failure, external forces, water, animals or foreign materials;
Products malfunction caused by disassembly or alter of components by customers or, products disassembled or repaired by persons or organizations unauthorized by MAS Elettronica, or altered in factory specifications, or configured or expanded with the components that are not provided or recognized by MAS Elettronica and the resulted damage in appearance or function;
Product failures caused by the software or system installed by customers or inappropriate settings of software or computer viruses;
Products purchased from unauthorized sales;
Warranty (including verbal and written) that is not made by MAS Elettronica and not included in the scope of our warranty should be fulfilled by the party who committed. MAS Elettronica has no any responsibility;

- Within the period of warranty, the freight for sending products from customers to MAS Elettronica should be paid by customers; the freight from MAS Elettronica to customers should be paid by us. The freight in any direction occurs after warranty period should be paid by customers.
- Please contact technical support if there is any repair request.

Note:

MAS Elettronica will not take any responsibility on the products sent back without the permission of the company

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