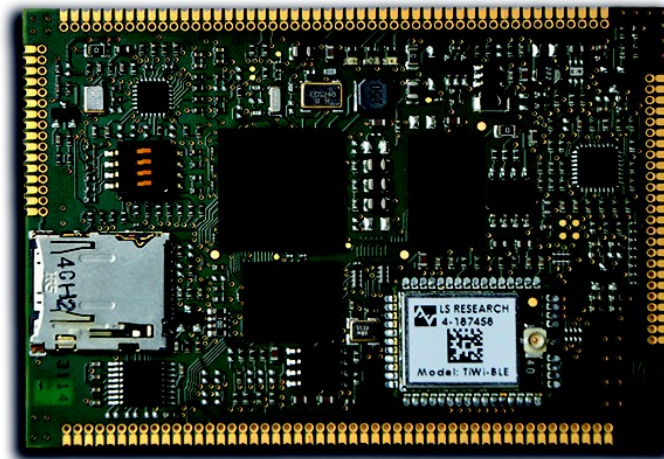


# GHITA IMX28x

## Standalone Embedded CPU Board Hardware Manual



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## ***Introduction***

The MCiMX28x module, based on the i.MX28 processor, offers a balanced ratio between computing and graphic performance.

The basis for this is an ARM926 core with up to 454 MHz. The realised memory on the module provides best system support.

The module is best suited for smart metering and control applications. It can be used with small and medium display. A large number of interfaces and module functions are implemented in the CPU due to the high level of interface and function integration.

This allows the basic board to be developed easily and at low-cost.

The module can be directly soldered on the carrier board in this way there is no need for board to board connectors.

All the processor's functional pins are routed to the edge connectors on the module.

Compatible products:

- Carrier Board MMST01 compatible with the the MCIMX28x adapter board.
- Carrier Board MMST02 compatible with the the MCIMX28x adapter board.
- Carrier Board MMST03 compatible with the the MCIMX28x adapter board.
- Carrier Board MMST04 compatible with the the MCIMX28x adapter board.

Operating systems support:

- Linux kernel 2.6.35, uboot 2008.09 and LTI 1.0.0  
([http://www.freescale.com/webapp/sps/site/prod\\_summary.jsp?code=IMX28\\_SW](http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=IMX28_SW))
- Qt embedded 4.7.4

## Features

The features of the IMX287 board are:

### Microprocessor

- i.MX287 (454 MHz)

### System interfaces

- Up to 1x Ethernet 10/100 Mbit
- Up to 2x CAN 2.0B
- Up to 4x UART
- 1x serial Debug
- 1x USB 2.0 high-speed HOST interface
- 1x USB 2.0 high-speed OTG interface
- 1x SDIO/MMC
- Up to 2x I2C
- Up to 2x SPI

### ADC

- Up to 8x 12 bit ADC channels (1x High Speed)

### Graphic

- 24 bit TFT Interface

### Audio

- Codec audio o I2S su connettore

### Memory

- DDR2-SDRAM: up to 256 MB

### Comunication

- 1x Wifi 802.11 b/g/n and Bluetooth BLE module

### Other

Real Time Clock (RTC)  
Temperature sensor  
CPU JTAG Interface  
Supervisor 3,3 V

## **GPIO**

- variable in number, shared with other devices

## **Power supply**

- 3,3V(optional); 5V(std)
- 500mW (operational) and 10mW(standby)

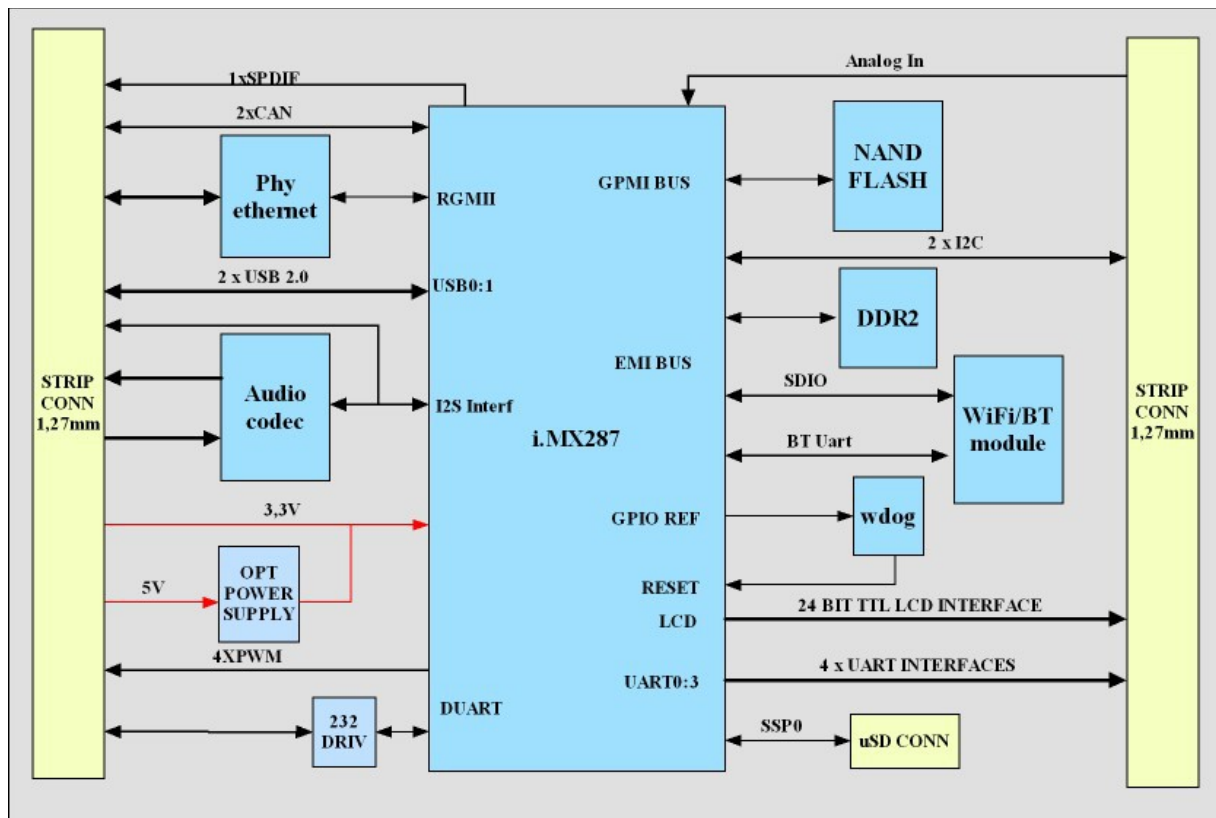
## **Ambient conditions**

- Standard temperature range: 0 °C...+70 °C
- Extended temperature range: -40 °C...+85 °C

## **Mechanical**

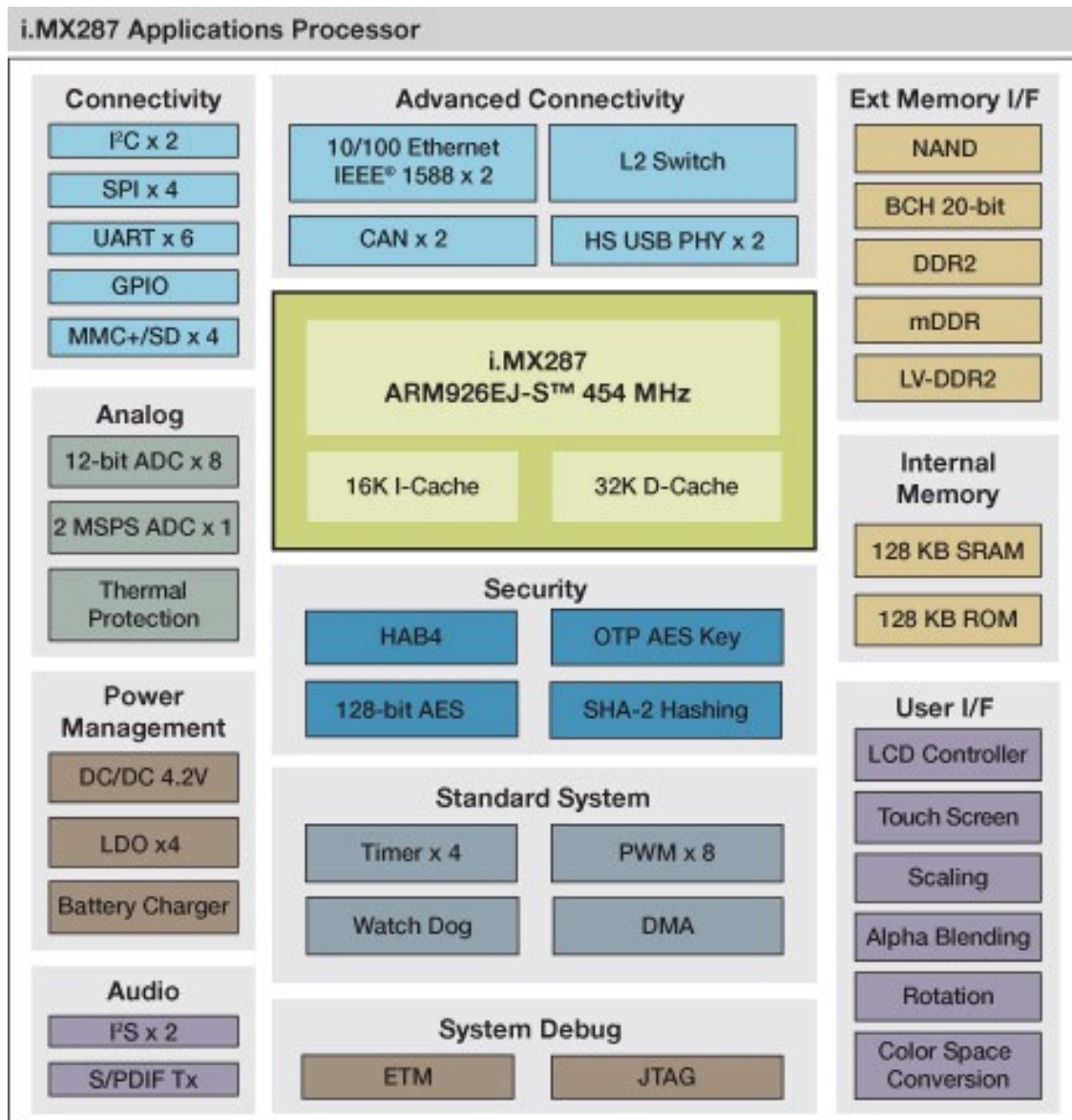
- 743 mm x 51.44 mm

## Board Block Diagram





## System Description



## CPU

The Freescale processor i.MX28 (MCIMX287CVM4B) based on an ARM926EJ-S™ core is produced in 90 nm technology. It provides a wide range of functions. Below is the processor block diagram:

## DDR2 Memory

The MCIMX28x supports up to 256Mbyte, 200Mhz 16 bit DDR2 SDRAM. For more info about the DDR2 SDRAM see the following table:

Manufacturer	Manufacturer's number	Type	Capacity	Temp. Range	Remark
Micron	Micron MT47H64M16H R-3IT	64M16	128 Mbyte	-40 to +85 °C	
Micron	MT47H64M16H R-25EIT:H	64M16	128 Mbyte	-40 to +85 °C	Default
Micron	MT47H128M16R T-25EIT	128M16	256 Mbyte	-40 to +85 °C	

## Nand Flash

The MCIMX28x is available with 256Mbyte (up to 4Gbyte) of NAND FLASH memory. The NAND flash is used for flash disk purposes, O.S. run-time-image and the bootloader (boot from NAND). First block (block address 00h) of the memory device is guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles). For more information about the Nand Flash devices see the following link:

<http://www.micron.com/parts/nand-flash/mass-storage/mt29f4g08abadawp-it>

## uSD Connector

The MCIMX28x contains an on board uSD connector supporting micro SD cards up to 192Mbit/sec (24MByte/sec) in High-Speed SD mode 4-bit data transfer. The CPU can boot from this device (MMC0). Extremely small size: Small external dimensions and the above-the-board height make the connectors the smallest on the market.

**Card detection switch:** The card detection switch is Normally Open

## LAN

The MCIMX28x has one Ethernet interface 10/100 Mbit/s Ethernet. For the Fast Ethernet interface the RMII interface has been used

## ***Fast Ethernet PHY***

The physical device used is the LAN8720A/LAN8720Ai is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards.

The LAN8720A/LAN8720Ai supports communication with an Ethernet MAC via a standard RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10Mbps(10BASE-T) and 100Mbps (100BASE-TX) operation. The LAN8720A/LAN8720Ai implements autonegotiation to automatically determine the best possible speed and duplex mode of operation. HPAuto-MDIX support allows the use of direct connect or cross-over LAN cables.

For more information about the LAN8720A/LAN8720Ai devices see the following link.

<http://ww1.microchip.com/downloads/en/DeviceDoc/8720a.pdf>

## ***Wifi module***

The TiWi-BLE module is a high performance 2.4 GHz IEEE 802.11 b/g/n and Bluetooth 2.1+EDR radio in a cost effective, pre-certified footprint. The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface. The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port. For more information about the TiWi-BLE module see the following link:

<http://www.lsr.com/downloads/products/330-0087.pdf>

## ***Touch Screen Controller***

The board has a 4 wire resistive Touch screen controller. It is directly connected to the processor's analog inputs. The analog signals are routed through the board to board connectors ready to be used for the touchscreen or simply analog inputs.

For more information see the Hardware reference manual.

[IMX28 hardware reference manual](#)

## Audio codec

Audio interfaces of MCIMX28x are featured by an on-board Freescale's feature-rich SGTL5000XNAA3 audio codec device. Please refer to the [data sheet](#) for detailed electrical characteristics of relevant interfaces.

The SGTL5000 is a Low Power Stereo Codec with Headphone Amp from Freescale, and is designed to provide a complete audio solution for products needing LINEIN, MIC\_IN, LINEOUT, headphone-out, and digital I/O.

## USB 2.0 High speed interface

The board has 2 USB 2.0 high speed interfaces, the signals are routed to the board to board connectors.

## System boot

The MCIMX28x can boot from uSD or from NAND flash. The selection is made through the dipswitch S1 present on the board.

Boot device	S1	S2	S3	S4
uSD	ON	OFF	OFF	ON
Nand flash	OFF	OFF	ON	OFF

## Power supply

The board must be powered through the board to board connector, the supply must be  $3,45V \pm 5\%$ .

## Absolute Maximum Rating

Power Supply	Min	Max	Unit
Main Power Supply, DC IN	0.3	3.6	V
Digital IOs: UARTs, LCD, MMC2, ISP, SPI, McBSP, I2C, GPMC, JTAG	-0.3	3.6	V
Analog IOs: AIN0-7	0.3	3.3	V

Table 1: Absolute Maximum Characteristics

## Operational Characteristics

### Power supplies

Power Supply	Min	Typical	Max	Unit
Main Power Supply, DC IN	-5%	5.0	+5%	V

Table 2: Power Supplies Operational Characteristics

### Power Consumption

Power Supply	Min	Typical	Max	Unit
Main Power Supply DC IN		0.5	0.8	W
Stand by mode		10		mW

Table 3: Power Consumption

## DC Electrical Characteristics

Parameter	Min	Typical	Max	Unit
<b>Digital IOs: UARTs, LCD, MMC2, ISP, SPI, McBSP, I2C, GPMC, JTAG</b>				
V <sub>IH</sub>	2			
V <sub>IL</sub>			0.8	V
V <sub>OH</sub>	DC-IN - 0.1			V
V <sub>OL</sub>			0.2	V
<b>Analog IOs: AIN0-7</b>				
V <sub>DC</sub>	0		3.3	V

•Table 4: DC Electrical Characteristics

## Environmental Specifications

Working Temperature Range	Min	Max
Commercial Operating Temperature	0°C	+70°C

Range		
Industrial Operating Temperature Range	-40°C	+85°C

Table 5: Environmental specifications

## I2C mapping

Information on I2C address assignments are provided below.

MCIMX28 Function	IMX28x I2C Port	Address
Audio Codec	I2C0	0001010

Table 6: I2C Bus Addresses

## LCD Controller

The IMX28x contains the LCDIF display controller module which connects to the AXI bus. High display resolutions up to 800x480 supported. 8/16/18/24 bit LCD data bus support available. Programmable timing and parameters for system, MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.

ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

For more informations [IMX28 hardware reference manual](#)

## CAN Interfaces

The i.MX28 includes dual FlexCAN2 controllers which are compatible with the CAN 2.0B protocol specification. The CAN Protocol Interface (CPI) manages the serial communication on the CAN bus, requesting RAM access for receiving and transmitting message frames, validating received messages and performing error handling. The Message Buffer Management (MBM) handles Message Buffer selection for reception and transmission, taking care of arbitration and ID matching algorithms.

For more informations [IMX28 hardware reference manual](#)

## Configuration Connector

### Connector J7 uSD

The J7 is the uSD connector, used for boot purposed and system upgrading. The pinout is standard.

### Connector J3

PIN	NAME	DIR	DESCRIPTION	LOGI C LEVE L	Alternate function on IMX28	IMX28 pin
1	5V	PWR	5V POWER RAIL			
2	5V	PWR	5V POWER RAIL			
3	5V	PWR	5V POWER RAIL			
4	GND	PWR	GND SIGNAL			
5	AUDIO_LIN_L_CONN	OUT	Audio Line out left channel	ANALO G		
6	AUDIO_LIN_R_CONN	OUT	Audio Line out right channel	ANALO G		
7	GND	PWR	GND SIGNAL			
8	HEADPHONE_LEFT	IN	MICROPHONE LEFT	ANALO G		
9	HEADPHONE_RIGHT	IN	MICROPHONE RIGHT	ANALO G		
10						
11	SPDIF_OUT_CONN		SPDIF AUDIO SIGNAL	ANALO G		
12	GND	PWR	GND SIGNAL			
13	HSADC0	IN	HIGH SPEED ADC CHANN	ANALO G		B14
14	LRADC6	IN	LOW RESOLUTION ADC CHANNEL 6	ANALO G		C14
15	LRADC5	IN	LOW RESOLUTION ADC CHANNEL 5	ANALO G		D15
16	LRADC4	IN	LOW RESOLUTION ADC CHANNEL 4	ANALO G		D13
17	LRADC3	IN	LOW RESOLUTION ADC CHANNEL 3	ANALO G		D9
18	LRADC2	IN	LOW RESOLUTION ADC CHANNEL 2	ANALO G		C8
19	LRADC1	IN	LOW RESOLUTION ADC CHANNEL 1	ANALO G		C9
20	LRADC0	IN	LOW RESOLUTION ADC CHANNEL 0	ANALO G		C15
21	GPIO2_24	I/O	AUART1_RX/SSP2_CARD_ DETECT/PWM_0/GPIO3_4	TTL 3,3V	SSP3_SCK/AUART4_TX/ENET 1_1588_EVENT0_OUT/GPIO2 _24	A2
22	GPIO2_25	I/O	GPIO	TTL 3,3V	SSP3_MOSI/SSP3_CMD/AUA RT4_RX/ENET1_1588_EVENT 0_IN/GPIO2_25	C2

23	GPIO2_26	I/O	GPIO	TTL 3,3V	SSP3_MOSI/SSP3_CMD/AUART4_RX/ENET1_1588_EVENT0_IN/GPIO2_25	B2
24	GPIO2_27	I/O	GPIO	TTL 3,3V	SSP3_SS0/SSP3_D3/AUART4_CTS/ENET1_1588_EVENT1_IN/GPIO2_27	D2
25	GND	PWR	GND SIGNAL			

## Connector J4

PI N	NAME	DIR	DESCRIPTION	LOGIC LEVEL	Alternate function on IMX28	IMX28 pin
1	GND	PWR	GND SIGNAL			
2	AUART0_RX	IN	UART0 RX SIGNAL	TTL 3,3V	AUART0_RX/I2C0_SCL/DUART_CTS/GPIO3_0	G5
3	AUART0_TX	OUT	UART0 TX SIGNAL	TTL 3,3V	AUART0_TX/I2C0_SDA/DUART_RTS/GPIO3_1	H5
4	AUART0_CTS	IN	UART0 CTS SIGNAL	TTL 3,3V	AUART0_CTS/AUART4_RX/DUART_RX/GPIO3_2	J6
5	AUART0_RTS	OUT	UART0 RTS SIGNAL	TTL 3,3V	AUART0_RTS/AUART4_TX/DUART_TX/GPIO3_3	J7
6	AUART1_RX	IN	UART1 RX SIGNAL	TTL 3,3V	AUART1_RX/SSP2_CARD_DETECT/PWM_0/GPIO3_4	L4
7	AUART1_TX	OUT	UART1 TX SIGNAL	TTL 3,3V	AUART1_TX/SSP3_CARD_DETECT/PWM_1/GPIO3_5	K4
8	AUART1_CTS	IN	UART1 CTS SIGNAL	TTL 3,3V	AUART1_CTS/USB0_OVERCURRENT/TIMROT_ROTARYA/GPIO3_6	K5
9	AUART1_RTS	OUT	UART1 RTS SIGNAL	TTL 3,3V	AUART1_RTS/USB0_ID/TIMROT_ROTARYB/GPIO3_7	J5
10	AUART2_RX	IN	UART2 RX SIGNAL	TTL 3,3V	AUART2_RX/SSP3_D1/SSP3_D4/GPIO3_8	F6
11	AUART2_TX	OUT	UART2 TX SIGNAL	TTL 3,3V	AUART2_TX/SSP3_D2/SSP3_D5/GPIO3_9	F5
12	GND	PWR	GND SIGNAL			
13	AUART3_RX	IN	UART3 RX SIGNAL	TTL 3,3V	AUART3_RX/CAN0_TX/ENET0_1588_EVENT0_OUT/GPIO3_12	M5
14	AUART3_TX	OUT	UART3 TX SIGNAL	TTL 3,3V	AUART3_TX/CAN0_RX/ENET0_1588_EVENT0_IN/GPIO3_13	L5
15	AUART3_CTS	IN	UART3 CTS SIGNAL	TTL 3,3V	AUART3_CTS/CAN1_TX/ENET0_1588_EVENT1_OUT/GPIO3_14	L6
16	AUART3_RTS	OUT	UART3 RTS SIGNAL	TTL 3,3V	AUART3_RTS/CAN1_RX/ENET0_1588_EVENT1_IN/GPIO3_15	K6
17	MANUAL_RESET#					
18	GPIO3_18	I/O	GPIO	TTL 3,3V	PWM2/USB0_ID/USB1_OVERCURRENT/GPIO3_18	K8
19	GPIO4_9	I/O	GPIO	TTL 3,3V	ENET0_RXD2/ENET1_RXD0/ENET0_1588_EVENT0_OUT/GPIO4_9	J1
20	GPIO4_10	I/O	GPIO	TTL 3,3V	ENET0_RXD3/ENET1_RXD1/ENET0_1588_EVENT0_IN/GPIO4_10	J2
21	GPIO4_11	I/O	GPIO	TTL 3,3V	ENET0_TXD2/ENET1_TXD0/ENET0_1588_EVENT1_OUT/GPIO4_11	G1
22	GPIO4_12	I/O	GPIO	TTL 3,3V	ENET0_TXD3/ENET1_TXD1/ENET0_1588_EVENT1_IN/GPIO4_12	G2
23	GPIO4_14	I/O	GPIO	TTL 3,3V	ENET0_COL/ENET1_TX_EN/ENET0_1588_EVENT3_OUT/GPIO4_14	J4



24	GPIO4_15	I/O	GPIO	TTL 3,3V	ENET0_CRIS/ENET1_RX_EN/ENET0_1588_EV ENT3_IN/GPIO4_15	J3
25	ENET_CLK	I/O	ETHERNET CLK	TTL 3,3V	ENET_CLK/GPIO4_16	E2
26	ENET_MDC	I/O	RMII CLK	TTL 3,3V	ENET0_MDC/GPI\MII\ \CIE\4\SAIF0_SDATA1/ GPIO4_0	G4
27	ENET_MDIO	I/O	RMII MDIO	TTL 3,3V	ENET0_MDIO/GPI\MII\ \CIE\5\SAIF0_SDATA2/ GPIO4_1	H4
28	I2C0_SCL	I/O	I20 CLOCK SIGNAL	TTL 3,3V	I2C0_SCL/TIMROT_ROTARYA/DUART_RX/GPIO3_2 4	C7
29	I2C0_SDA	I/O	I20 DATA SIGNAL	TTL 3,3V	I2C0_SDA/TIMROT_ROTARYB/DUART_TX/GPIO3_2 5	D8
30	GND	PWR	GND SIGNAL			
31	I2C1_SCL	I/O	I20 CLOCK SIGNAL	TTL 3,3V	AUART2_CTS/I2C1_SCL/SAIF1_BITCLK/GPIO3_10	H6
32	I2C1_SDA	I/O	I20 DATA SIGNAL	TTL 3,3V	AUART2_RTS/I2C1_SDA/SAIF1_LRCLK/GPIO3_11	H7
33	SSP2_SCK	OUT	SDIO interface available when WIFI is not mounted	TTL 3,3V	SSP2_SCK/AUART2_RX/SAIF0_SDATA1/GPIO2_16	A3
34	SSP2_CMD	OUT	SDIO interface available when WIFI is not mounted	TTL 3,3V	SSP2_MOSI/SSP2_CMD/AUART2_TX/SAIF0_SDATA 2/GPIO2_17	C3
35	SSP2_D0	I/O	SDIO interface available when WIFI is not mounted	TTL 3,3V	SSP2_MISO/SSP2_D0/AUART3_RX/SAIF1_SDATA1/ GPIO2_18	B3
36	SSP2_D3	I/O	SDIO interface available when WIFI is not mounted	TTL 3,3V	SSP2_SS0/SSP2_D3/AUART3_TX/SAIF1_SDATA2/G PIO2_19	C4
37	SSP2_D1	I/O	SDIO interface available when WIFI is not mounted	TTL 3,3V	SSP2_SS1/SSP2_D4/SSP2_D1/USB1_OVERCURRE NT/GPIO2_20	D3
38	SSP2_D2	I/O	SDIO interface available when WIFI is not mounted	TTL 3,3V	SSP2_SS1/SSP2_D4/SSP2_D1/USB1_OVERCURRE NT/GPIO2_20	D4
39	GPIO2_12	I/O	GPIO	TTL 3,3V	SSP1_SCK/SSP2_D1/ENET0_1588_EVENT2_OUT/G PIO2_12	B1
40	GPIO2_13	I/O	GPIO	TTL 3,3V	SSP1_CMD/SSP2_D2/ENET0_1588_EVENT2_IN/GPI O2_13	C1
41	GPIO2_14	I/O	GPIO	TTL 3,3V	SSP1_DATA0/SSP2_D6/ENET0_1588_EVENT3_OUT /GPIO2_14	D1
42	GPIO2_15	I/O	GPIO	TTL 3,3V	SSP1_DATA3/SSP2_D7/ENET0_1588_EVENT3_IN/G PIO2_15	E1
43	GPIO0_23	I/O	GPIO	TTL 3,3V	GPMI_RDY3/CAN0_RX/HSADC_TRIGGER/GPIO0_2 3	L8
44	GPIO0_22	I/O	GPIO	TTL 3,3V	GPMI_RDY2/CAN0_TX/ENET0_TX_ER/GPIO0_22	M8
45	GPIO0_21	I/O	GPIO	TTL 3,3V	GPMI_RDY1/SSP1_CMD/GPIO0_21	N8

46	GND	PWR	GND SIGNAL		
47	TXP0	OUT	ETHERNET TXP SIGNAL	ECL	
48	TXN0	OUT	ETHERNET TXN SIGNAL	ECL	
49	RXP0	IN	ETHERNET RXP SIGNAL	ECL	
50	RXN0	IN	ETHERNET RXN SIGNAL	ECL	

## Connector J5

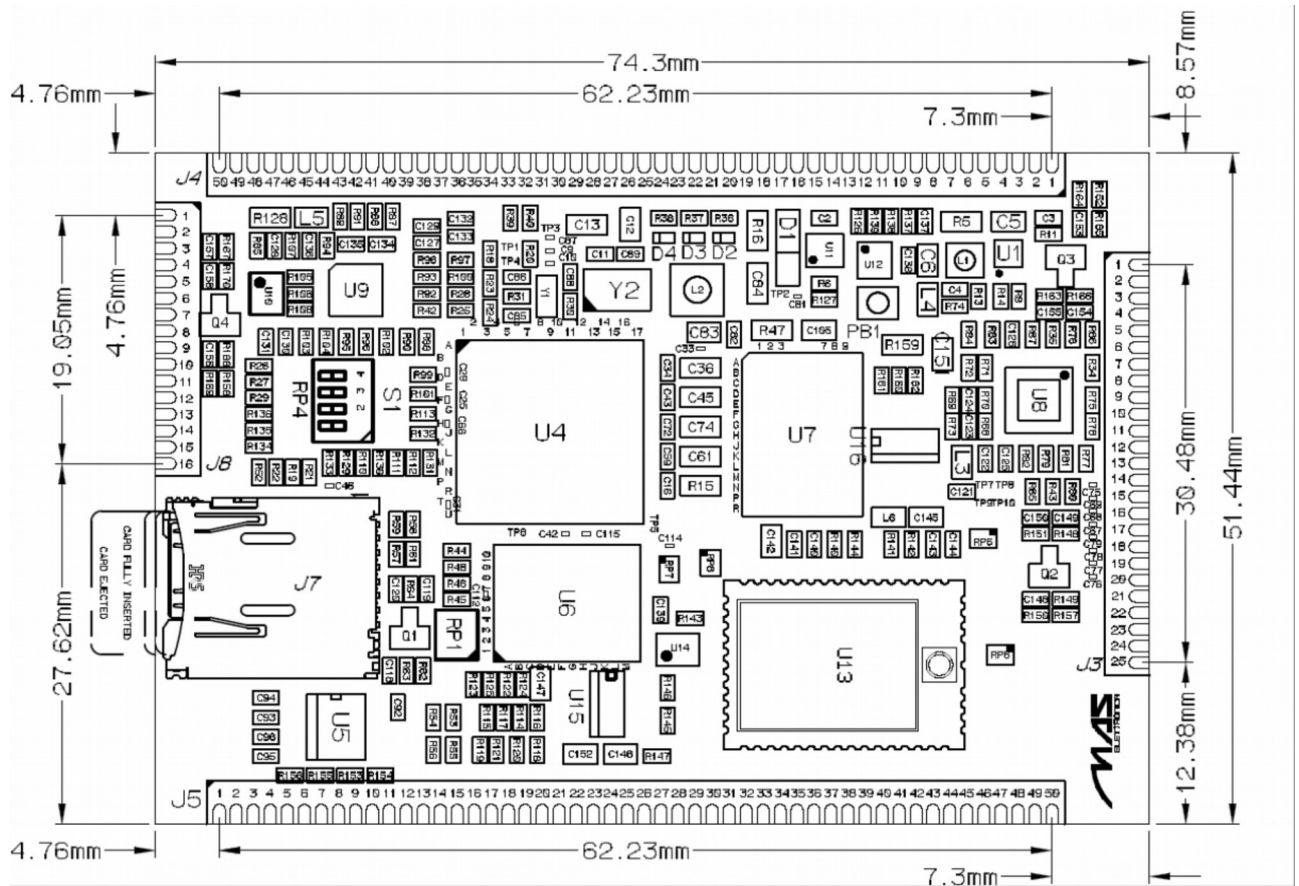
PIN	NAME	DIR	DESCRIPTION	LOGIC LEVEL	Alternate function on IMX28	IMX2 8 pin
1	GND	PWR	GND SIGNAL			
2	LCD_ENABLE	OUT	LCD ENALBLE SIGNAL	TTL 3,3V	LCD_CS/LCD_ENABLE/GPIO1_27	P5
3	LCD_DOTCLK	OUT	LCD DOTCLK SIGNAL	TTL 3,3V	LCD_RS/LCD_DOTCLK/GPIO1_26	M4
4	LCD_HSYNC	OUT	LCD HSYNC SIGNAL	TTL 3,3V	LCD_WR_RWN/LCD_HSYNC/ETM_TCLK/GPIO1_25	K1
5	LCD_VSYNC	OUT	LCD VSYNC SIGNAL	TTL 3,3V	LCD_WR_RWN/LCD_HSYNC/ETM_TCLK/GPIO1_25	P4
6	LCD_D23	OUT	LCD D23 SIGNAL	TTL 3,3V	LCD_D23/ENET1_1588_EVENT3_IN/ETM_DA0/GPIO1_23	R5
7	LCD_D22	OUT	LCD D22 SIGNAL	TTL 3,3V	LCD_D22/ENET1_1588_EVENT3_OUT/ETM_DA1/GPIO1_22	T5
8	LCD_D21	OUT	LCD D21 SIGNAL	TTL 3,3V	LCD_D21/ENET1_1588_EVENT2_IN/ETM_DA2/GPIO1_21	U5
9	LCD_D20	OUT	LCD D20 SIGNAL	TTL 3,3V	LCD_D20/ENET1_1588_EVENT2_OUT/ETM_DA3/GPIO1_20	R4
10	LCD_D19	OUT	LCD D19 SIGNAL	TTL 3,3V	LCD_D19/ETM_DA4/GPIO1_19	T4
11	LCD_D18	OUT	LCD D18 SIGNAL	TTL 3,3V	LCD_D18/ETM_DA5/GPIO1_18	U4
12	LCD_D17	OUT	LCD D17 SIGNAL	TTL 3,3V	LCD_D17/ETM_DA6/GPIO1_17	R3
13	GND	PWR	GND SIGNAL			
14	LCD_D16	OUT	LCD D16 SIGNAL	TTL 3,3V	LCD_D16/ETM_DA7/GPIO1_16	T3
15	LCD_D15	OUT	LCD D15 SIGNAL	TTL 3,3V	LCD_D15/ETM_DA15/GPIO1_15	U3
16	LCD_D14	OUT	LCD D14 SIGNAL	TTL 3,3V	LCD_D14/ETM_DA14/GPIO1_14	U2
17	LCD_D13	OUT	LCD D13 SIGNAL	TTL 3,3V	LCD_D13/ETM_DA13/GPIO1_13	T2
18	LCD_D12	OUT	LCD D12 SIGNAL	TTL 3,3V	LCD_D12/ETM_DA12/GPIO1_12	T1
19	LCD_D11	OUT	LCD D11 SIGNAL	TTL 3,3V	LCD_D11/ETM_DA11/GPIO1_11	R2
20	LCD_D10	OUT	LCD D10 SIGNAL	TTL 3,3V	LCD_D10/ETM_DA10/GPIO1_10	R1
21	LCD_D09	OUT	LCD D09 SIGNAL	TTL 3,3V	LCD_D09/ETM_DA9/ETM_DA4/GPIO1_9	P3
22	LCD_D08	OUT	LCD D08 SIGNAL	TTL 3,3V	LCD_D08/ETM_DA8/ETM_DA3/GPIO1_8	P2
23	LCD_D07	OUT	LCD D07 SIGNAL	TTL 3,3V	LCD_D07/ETM_DA7/GPIO1_7	P1
24	LCD_D06	OUT	LCD D06 SIGNAL	TTL 3,3V	LCD_D06/ETM_DA6/GPIO1_6	N2
25	LCD_D05	OUT	LCD D05 SIGNAL	TTL 3,3V	LCD_D05/ETM_DA5/GPIO1_5	M3

26	LCD_D04	OUT	LCD D04 SIGNAL	TTL 3,3V	LCD_D04/ETM_DA4/ETM_DA9/GPIO1_4	M2
27	LCD_D03	OUT	LCD D03 SIGNAL	TTL 3,3V	LCD_D03/ETM_DA3/ETM_DA8/GPIO1_3	L3
27	LCD_D03	OUT	LCD D03 SIGNAL	TTL 3,3V	LCD_D03/ETM_DA3/ETM_DA8/GPIO1_3	L3
28	LCD_D02	OUT	LCD D02 SIGNAL	TTL 3,3V	LCD_D02/ETM_DA2/GPIO1_2	L2
29	LCD_D01	OUT	LCD D01 SIGNAL	TTL 3,3V	LCD_D01/ETM_DA1/GPIO1_1	K3
30	GND	PWR	GND SIGNAL			
31	LCD_D00	OUT	LCD D00 SIGNAL	TTL 3,3V	LCD_D00/ETM_DA0/GPIO1_0	K2
32	GPIO1_31	I/O	GPIO	TTL 3,3V	LCD_ENABLE/GPIO1_31	N5
33	GPIO3_30	I/O	GPIO	TTL 3,3V	LCD_RESET/LCD_VSYNC/GPIO3_30	M6
34	GPIO1_30	I/O	GPIO	TTL 3,3V	LCD_DOTCLK/SAIF1_MCLK /ETM_TCLK/GPIO1_30	N1
35	GPIO1_29	I/O	GPIO	TTL 3,3V	LCD_HSYNC/SAIF1_SDATA1/ETM_TCTL/GPIO 1_29	M1
36	GPIO1_28	I/O	GPIO	TTL 3,3V	LCD_VSYNC/SAIF1_SDATA0/GPIO1_28	L1
37	SAIF0_MCLK	OUT	AVAILABLE ONLY IF CODEC IS NOT EQUIPPED	TTL 3,3V	SAIF0_MCLK/PWM_3/AUART4_CTS/GPIO3_20	G7
38	SAIF0_LRCLK	OUT	AVAILABLE ONLY IF CODEC IS NOT EQUIPPED	TTL 3,3V	SAIF0_LRCLK/PWM_4/AUART4_RTS/GPIO3_2 1	G6
39	SAIF0_BITCLK	OUT	AVAILABLE ONLY IF CODEC IS NOT EQUIPPED	TTL 3,3V	SAIF0_BITCLK/PWM_5/AUART4_RX/GPIO3_22	F7
40	SAIF0_SDATA0	IN	AVAILABLE ONLY IF CODEC IS NOT EQUIPPED	TTL 3,3V	SAIF0_SDATA0/PWM_6/AUART4_TX/GPIO3_23	E7
41	SAIF0_SDATA1	OUT	AVAILABLE ONLY IF CODEC IS NOT EQUIPPED	TTL 3,3V	SAIF1_SDATA0/PWM_7/SAIF0_SDATA1/GPIO3 _26	E8
42	NA					
43	BACKLIGHT_PWM			TTL 3,3V	PWM4/GPIO3_29	E10
44	WL_EN		Available when WIFI not equipped	TTL 3,3V	SSP0_DATA6/SSP2_CMD/GPIO2_6	D5
45	WLAN_IRQ		Available when WIFI not equipped	TTL 3,3V	SSP0_DATA7/SSP2_SCK/GPIO2_7	B4
46	GND	PWR	GND SIGNAL			
47	USB_0_DM	I/O	USB 0 NEG SIGNAL			A10
48	USB_0_DP	I/O	USB 0 POS SIGNAL			B10
49	USB_1_DM	I/O	USB 1 NEG SIGNAL			B8

## Connector J8

PIN	NAME	DIR	DESCRIPTION	LOGIC LEVEL	Alternate function on IMX28	IMX28 pin
1	3V3	PWR	3V3 POWER RAIL			
2	3V3	PWR	3V3 POWER RAIL			
3	JTAG_TMS	IN	JTAG TEST MODE SIGNAL	TTL 3,3V		D12
4	JTAG_TCK	OUT	JTAG CLOCK SIGNAL	TTL 3,3V		E11
5	JTAG_TDI	IN	JTAG DATA IN SIGNAL	TTL 3,3V		E12
6	JTAG_TDO	OUT	JTAG DATA OUT SIGNAL	TTL 3,3V		E13
7	JTAG_TRST	IN	JTAG RESET SIGNAL	TTL 3,3V		D14
8	JTAG_RTCK	OUT	JTAG RT CLOCK SIGNAL	TTL 3,3V		E14
9	RESETN	IN	RESET INPUT	TTL 3,3V		A14
10	PSWITCH	IN	POWER ON SIGNAL	TTL 3,3V		A11
11	ENET0_LINKLED1	OUT	ETHERNET LINK LED	TTL 3,3V		
12	ENET0_100MLED2	OUT	ETHERNET SPEED LED	TTL 3,3V		
13	TX_DEBUG_232	OUT	DEBUG TX SERIAL	RS232		
14	RX_DEBUG_232	IN	DEBUG RX SERIAL	RS232		
15	GND	PWR	GND SIGNAL			
16	GND	PWR	GND SIGNAL			

## Board Layout



## **Rohs compliance**

The MCAM335x Standalone Embedded CPU Board comply with the European Union's Directive 2002/95/EC: "Restrictions of Hazardous Substances".

## **Warranty Terms**

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