Dory iMX6UL
Module
Rev 1.0

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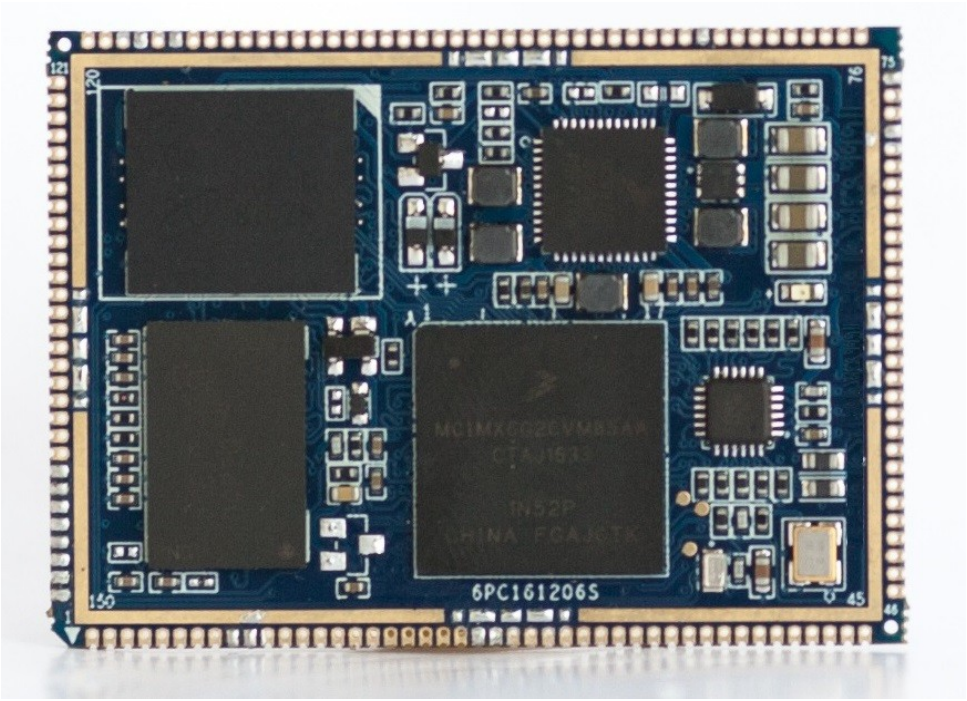

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Revision History..

Rev.	Document Code	Released	Written	Verified	Approved
1.0	Dory iMX6UL	02/8/2017	S.Mascetti	02/8/2017	S.Mascetti

Introduction

The DORY CPU is IMX6UL and IMX6ULL general purpose system on module designed to work in Industrial, Automotive and consumer environment.
The DORY CPU is an SMT module with a small foot print ready to be solder on the Application Board (Carrier Board).

Reference Documentation

1) IPC-A-610E Acceptability of Electronics Assemblies Training and Certification Program
2) IPC-A-600 Acceptability of Printed Boards Training and Certification Program
3) IPC-A-6011: Generic Performance Specification for Printed Boards
4) IPC-A-6012D: Qualification and Performance Specification for Rigid Printed Boards
5) RoHS II Directive 2011/65/EU and 2015/863/EU (2002/95/EC and successive amendments)
6) REACH - Regulation (EC) No. 1907/2006
7) NXP - iMX6UL Datasheet and Application Notes
8) NXP - PF3000 DataSheet and Application Notes

Specification

Mechanical

DORY CPU PCB Board Dimensions : 48,72 x 35mm x1.2(*)

Electrical

DORY CPU Processor Board : (+5Vdc +/- 5%) or +4Vdc (LiIon Cell)

Temperature

The working temperature is -40°C to +85°C.
The storage temperature is -40°C to +85°C.

Certifications

European CE Mark

The DORY CPU product is CE compliant

The CE mark indicate that the product is compliant to all the European Community Directive. MAS Elettronica is not liable about the use of their products associated to other devices not CE Compliant and not compliant with the technical requirements of this document.

RoHS and REACH Directive

This product (include all the components, materials for packaging, etc.) must be compliant with the RoHS European directive 2002/95/CE (known as RoHS, Restriction on the use of certain Hazardous Substances) for the use of particular dangerous material on electrical equipment (AEE)

RoHS Directive 2011/65/EU
EN 50581:2012
EN 62321:2009
REACH Regulation (EC) No 1907/2006

DORY CPU

The DORY CPU is the system on module based on NXP iMX6UL family that integrate the following peripherals / functions:

- NXP i.MX6UL Application Processor
- 512MiB or 1GiB of DDR3L Memory
- 4/8/16GB of eMMC Flash
- Real Time Clock
- LCD Interface (24Bit) (Optionally con be configured as General Purpose TTL 3V3 I/O)
- 3 Analog Input
- General Purpose I/O
- 6 UART Serial Port TTL 3V3 (RX - TX)
- 2 CAN Port TTL 3V3 with Driver Enable I/O
- 1 I2C Bus TTL 3V3
- 2 SPI Bus TTL 3V3
- SDIO Bus TTL 3V3
- I2S Bus
- 1 USB OTG Port
- 1 USB 2.0 Port
- 1 10/100 Ethernet Port with physical on board
- 1 10/100 Ethernet MAC Port

DORY CPU Operating System

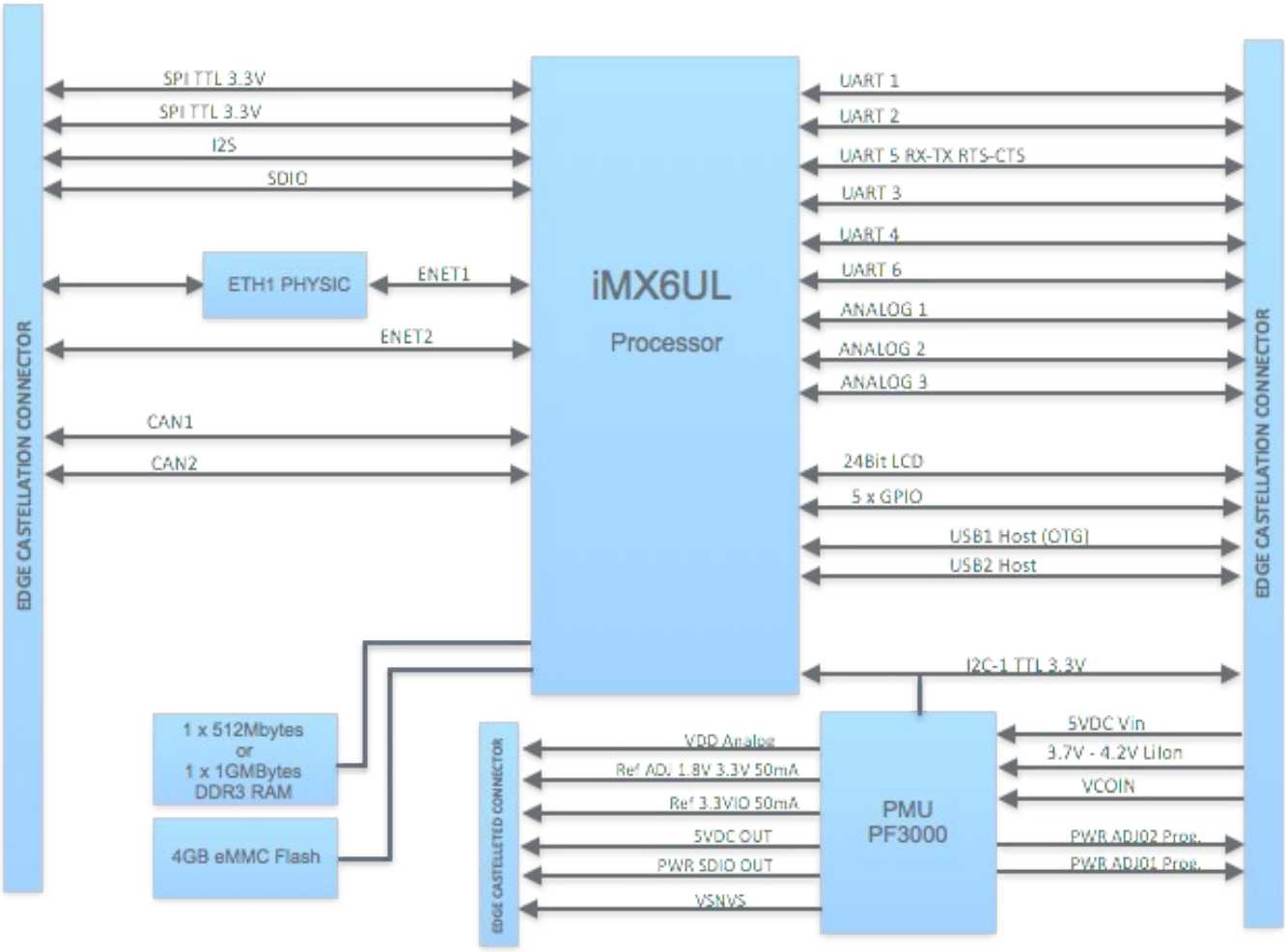
LINUX Kernel Version 4.1.15 or later build with YOCTO

Absolute Max ratings

Vin	5V DC
I max	300mA

Block Diagram

The DORY CPU block diagram is shown below:



Functionalities

Function	Type	Description
MEMORY	DDR3L Memory	The module is designed in order to support the following memory size/configuration: 512MiB 1*512MB DDR3L 1GiB 1*1GiB DDR3L
	eMMC Flash	The main FLASH memory of the module is an eMMC. The minimum size is 4/8/16GB. *On the eMMC are installed the Linux OS and uBoot.*
COMs	UART1 (Console)	This UART is used to communicate with the Linux Console TTL 3V3
	UART2--3-4-6	This UARTs are available as RX and TX TTL 3v3 UART. The RS232 driver should be added on the Application Board. These UARTs could be used as RS485 or RS422 adding the transceiver into the Application Board and using the GPIO to drive the data direction
	UART5	This UART is available RX, TX, CTS and RTS TTL 3V3. The UART5 could be used to connect devices that are using RTS and CTS (example BT Modules).
	Ethernet	The iMX6UL processor integrate 2 Ethernet Controller ETH0 and ETH1. The Physical Driver for ETH0 are present on the DORY CPU, and on the Castellated Connectors there are available the Signals to connect the Magnetic and RJ45. Link and activity LED signals are present in the Castellated Connector The MAC signal of ETH1 are available on the Castellated Connector. The Physical Driver have to be added on the Application Board in case the second ETH is required. *The MDx pins of ETH1 pins can be configured as GPIO.* *The MC Bus to configure the Physicals is shared between ETH0 and ETH1 MAC Controllers*
	CAN Port	2 CAN Port are provided by the iMX6UL processor. The CAN RX / TX are TTL 3V3 and the CAN Driver is not present on the board.
Expansin BUS	SDIO	The SDIO Bus function is provided by the iMX6UL Processor. This Bus can be used to connect a Flash Memory Card or other devices that are using this kind of communication Bus (example combo WIFI and BT Module). *The SDIO Bus could be 3V3 or TTL 1.8V Voltage level selectable on PMU PF3000.*
	I2S	The I2S bus function is provided by the iMX6UL Processor. *The signals are TTL 3V3 level and can be software configured as GPIO*
	SPI	2 SPI bus, SPI0 and SPI1,are available on the Castellated Connector. The Bus are TTL 3V3
	I2C	1 I2C bus is available on the Castellated Connector The Bus are TTL 3V3 The internal PMU PF3000 is connected on this I2C2 Bus.
Digital & AnalogI I/O	LCD/GPIO	An 24Bit LCD controller is present on the iMX6UL5 Processor. *If the LCD Function is not used the pins can be software configured as GPIO. The voltage level is configurable from 1.8V and 3.3V on PMU PF3000*
	ANALOG	3 Analog Input are present on the iMX6UL Processor. The voltage Input level is 3.3VMax *These pins can be software configured as GPIO*
USB	USB1	This port is an USB2.0 OTG Device/Host Mode.
	USB0	This port is an USB2.0 Host Only Mode and does not have a 5V power over current protection
	RTC	The Real Time Clock function is integrated on the iMX6UL Processor. Battery Back-up have to be provided on the Application Board
	PMU	The Power Management is performed by the PF3000.

Pin Definition

In the Embedded Processor Module all the signals are available on the Edge Castellated Connector.
The below table report:

- SoM Pin: draft of the Castellated Pin connector number;
- Label: the SoM pin name;
- Function: related CPU function;
- CPU pin: the CPU pin package;
- Power Domain: power rail connection;
- 2nd: second function available yes or no;
- 2nd Function: related CPU GPIO.

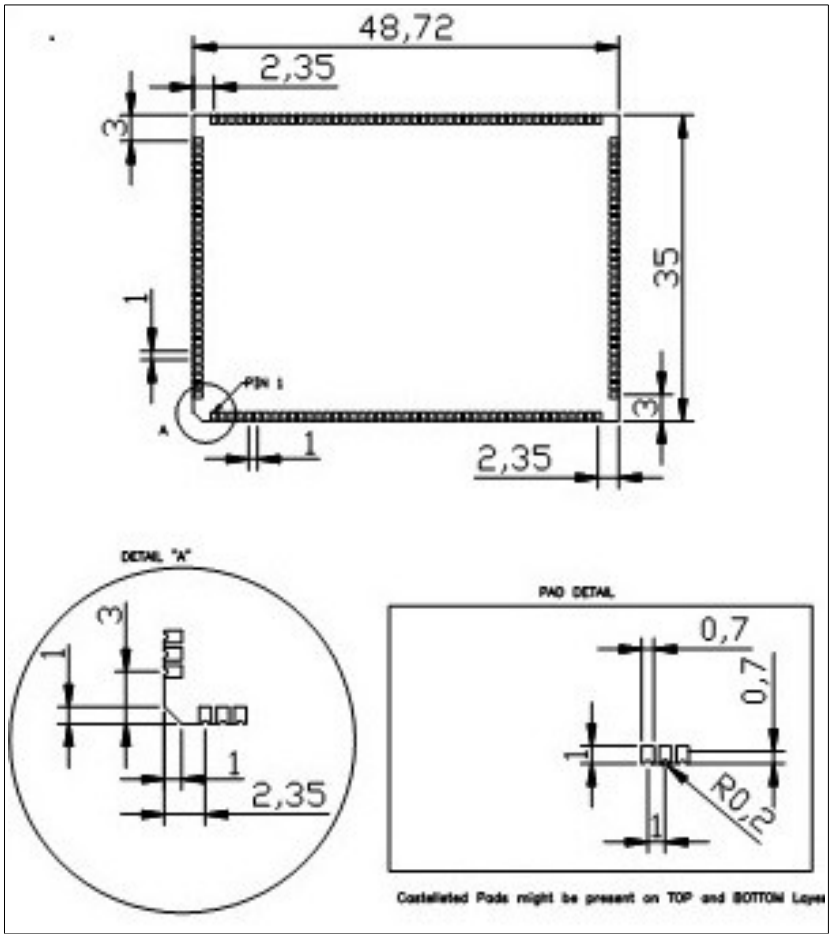
Primary Pin OUT

SoM Pin	Label	Function	Cpu Pin	Power	2nd	2nd Funcion
1	PWR_5V_IN	PF3000_VPWR				
2	PWR_5V_IN	PF3000_VPWR				
3	PWR_5V_IN	PF3000_VPWR				
4	PWR_5V_OUT	PF3000_VPWR_OUT*				
5	PWR_5V_OUT	PF3000_VPWR_OUT*				
6	PWR_5V_OUT	PF3000_VPWR_OUT*				
7	PWR_4V2_IN	PF3000_VIN				
8	PWR_4V2_IN	PF3000_VIN				
9	PWR_4V2_IN	PF3000_VIN				
10	PWR_IN_GND	PF3000_GND_VIN				
11	PWR_IN_GND	PF3000_GND_VIN				
12	PWR_IN_GND	PF3000_GND_VIN				
13	PWR_LiCELL_IN	PF3000_LICELL				
14	PWR_PERI01_OUT	PF3000_SW1AFB_3V3				
15	PWR_PERI02_OUT	PF3000_SW2FB_ADJ				
16	PWR_SDIO_OUT	PF3000_VCC_SD_ADJ				
17	PWR_VSNVS_OUT	SOM_VSNVS*				
18	PWR_ADC_OUT	PF3000_VLDO1_3V3*				
19	PWR_ADC_GND	PF3000_GND_OUT*				
20	PWR_DCDC5V_OUT	PF3000_SWBST_5V				
21	PWR_DCDC5V_GND	PF3000_GND_OUT				
22	PWR_ADJ01_OUT	PF3000_VLDO3_ADJ				
23	PWR_ADJ0X_GND	PF3000_GND_OUT				
24	PWR_ADJ02_OUT	PF3000_VLDO4_ADJ				
25	SYS_RESET_IN	SOM_RESET_IN				
26	SYS_RESET_OUT	SOM_RESET_OUT				
27	SYS_ON_OFF	SOM_ON_OFF				
28	ADC	ADC1_IN2(ADC1,adc_in2)	L14	PWR_PERI01_OUT	yes	gpio1_IO2(GPIO1,gpio_io,2)
29	ADC	ADC1_IN3(ADC1,adc_in3)	L17	PWR_PERI01_OUT	yes	gpio1_IO3(GPIO1,gpio_io,3)
30	ADC	ADC1_IN5(ADC1,adc_in5)	M17	PWR_PERI01_OUT	yes	gpio1_IO5(GPIO1,gpio_io,5)
31	BOOT	src_BOOT_MODE0(SRC,src_boot_mode,0)	T10	PWR_PERI01_OUT	yes	src_BOOT_MODE0(SRC,src_boot_mode,0)
32	BOOT	src_BOOT_MODE1(SRC,src_boot_mode,1)	U10	PWR_PERI01_OUT	yes	src_BOOT_MODE1(SRC,src_boot_mode,1)
33	CAN1	can1_TX(FLEXCAN1,can_tx)	H15	PWR_PERI01_OUT	yes	gpio1_IO26(GPIO1,gpio_io,26)
34	CAN1	can1_RX(FLEXCAN1,can_rx)	G14	PWR_PERI01_OUT	yes	gpio1_IO27(GPIO1,gpio_io,27)
35	CAN2	can2_TX(FLEXCAN2,can_tx)	J15	PWR_PERI01_OUT	yes	gpio1_IO22(GPIO1,gpio_io,22)
36	CAN2	can2_RX(FLEXCAN2,can_rx)	H14	PWR_PERI01_OUT	yes	gpio1_IO23(GPIO1,gpio_io,23)
37	GND					
38	ECSPI1	ecspi1_SCLK(ECSPI1,ecspi_sclk)	D4	PWR_PERI01_OUT	yes	gpio4_IO25(GPIO4,gpio_io,25)
39	ECSPI1	ecspi1_SS0(ECSPI1,ecspi_ss,0)	D3	PWR_PERI01_OUT	yes	gpio4_IO26(GPIO4,gpio_io,26)
40	ECSPI1	ecspi1_MOSI(ECSPI1,ecspi_mosi)	D2	PWR_PERI01_OUT	yes	gpio4_IO27(GPIO4,gpio_io,27)
41	ECSPI1	ecspi1_MISO(ECSPI1,ecspi_miso)	D1	PWR_PERI01_OUT	yes	gpio4_IO28(GPIO4,gpio_io,28)
42	GND					

43	ECSPI2	ecspi2_SCLK(ECSPI2,ecspi_sclk)	E4	PWR_PERI01_OUT	yes	gpio4_IO21(GPIO4,gpio_io,21)
44	ECSPI2	ecspi2_SS0(ECSPI2,ecspi_ss,0)	E3	PWR_PERI01_OUT	yes	gpio4_IO22(GPIO4,gpio_io,22)
45	ECSPI2	ecspi2_MOSI(ECSPI2,ecspi_mosi)	E2	PWR_PERI01_OUT	yes	gpio4_IO23(GPIO4,gpio_io,23)
46	ECSPI2	ecspi2_MISO(ECSPI2,ecspi_miso)	E1	PWR_PERI01_OUT	yes	gpio4_IO24(GPIO4,gpio_io,24)
47	ECSPI2	ePCI		nc		nc
48	ECSPI2	ePCI		nc		nc
49	GND	GND				
50	ENET1_2	enet1_MDIO(ENET1,enet_mdio)	K17	PWR_PERI01_OUT		no
51	ENET1_2	enet1_MDC(ENET1,enet_mdc)	L16	PWR_PERI01_OUT		no
52	GND	GND				
53	ENET2	enet2_RDATA0(ENET2,enet_rdata,0)	C17	PWR_PERI01_OUT	yes	gpio2_IO8(GPIO2,gpio_io,8)
54	ENET2	enet2_RDATA1(ENET2,enet_rdata,1)	C16	PWR_PERI01_OUT	yes	gpio2_IO9(GPIO2,gpio_io,9)
55	ENET2	enet2_RX_EN(ENET2,enet_rx_en)	B17	PWR_PERI01_OUT	yes	gpio2_IO10(GPIO2,gpio_io,10)
56	ENET2	enet2_RX_ER(ENET2,enet_rx_er)	D16	PWR_PERI01_OUT	yes	gpio2_IO15(GPIO2,gpio_io,15)
57	ENET2	enet2_TX_CLK(ENET2,enet_tx_clk)	D17	PWR_PERI01_OUT	yes	gpio2_IO14(GPIO2,gpio_io,14)
58	ENET2	enet2_TDATA0(ENET2,enet_tdata,0)	A15	PWR_PERI01_OUT	yes	gpio2_IO11(GPIO2,gpio_io,11)
59	ENET2	enet2_TDATA1(ENET2,enet_tdata,1)	A16	PWR_PERI01_OUT	yes	gpio2_IO12(GPIO2,gpio_io,12)
60	ENET2	enet2_TX_EN(ENET2,enet_tx_en)	B15	PWR_PERI01_OUT	yes	gpio2_IO13(GPIO2,gpio_io,13)
61	ENET2	gpio5_IO6(GPIO5,gpio_io,6)	N11	PWR_VSNVS_OUT	yes	gpio5_IO6(GPIO5,gpio_io,6)
62	GND	GND				
63	GPIO_10	gpio1_IO10(GPIO1,gpio_io,10)	P15	PWR_PERI01_OUT	yes	gpio1_IO10(GPIO1,gpio_io,10)
64	GPIO_04	gpio5_IO3(GPIO5,gpio_io,3)	P10	PWR_VSNVS_OUT	yes	gpio5_IO3(GPIO5,gpio_io,3)
65	GPIO_03	gpio5_IO2(GPIO5,gpio_io,2)	P11	PWR_VSNVS_OUT	yes	gpio5_IO2(GPIO5,gpio_io,2)
66	GPIO_02	gpio5_IO1(GPIO5,gpio_io,1)	R9	PWR_VSNVS_OUT	yes	gpio5_IO1(GPIO5,gpio_io,1)
67	GPIO_01	gpio5_IO0(GPIO5,gpio_io,0)	R10	PWR_VSNVS_OUT	yes	gpio5_IO0(GPIO5,gpio_io,0)
68	I2C2	i2c2_SCL(I2C2,i2c_scl)	F3	PWR_PERI01_OUT	yes	gpio4_IO20(GPIO4,gpio_io,20)
69	I2C2	i2c2_SDA(I2C2,i2c_sda)	F2	PWR_PERI01_OUT	yes	gpio4_IO19(GPIO4,gpio_io,19)
70	I2S	sai2_RX_DATA(SAI2,sai_rx_data)	M14	PWR_PERI01_OUT	yes	gpio1_IO14(GPIO1,gpio_io,14)
71	I2S	sai2_TX_BCLK(SAI2,sai_tx_bclk)	N16	PWR_PERI01_OUT	yes	gpio1_IO13(GPIO1,gpio_io,13)
72	I2S	sai2_TX_SYNC(SAI2,sai_tx_sync)	N15	PWR_PERI01_OUT	yes	gpio1_IO12(GPIO1,gpio_io,12)
73	I2S	sai2_MCLK(SAI2,sai_mclk)	P14	PWR_PERI01_OUT	yes	gpio1_IO11(GPIO1,gpio_io,11)
74	I2S	sai2_TX_DATA(SAI2,sai_tx_data)	N14	PWR_PERI01_OUT	yes	gpio1_IO15(GPIO1,gpio_io,15)
75	GND	GND				
76	LCD	lcdif_WR_RWN(LCDIF,lcdif_wr_rwn)	A8	PWR_PERI02_OUT	yes	gpio3_IO0(GPIO3,gpio_io,0)
77	LCD	lcdif_DATA0(LCDIF,lcdif_data,0)	B9	PWR_PERI02_OUT	yes	gpio3_IO5(GPIO3,gpio_io,5)
78	LCD	lcdif_DATA1(LCDIF,lcdif_data,1)	A9	PWR_PERI02_OUT	yes	gpio3_IO6(GPIO3,gpio_io,6)
79	LCD	lcdif_DATA2(LCDIF,lcdif_data,2)	E10	PWR_PERI02_OUT	yes	gpio3_IO7(GPIO3,gpio_io,7)
80	LCD	lcdif_DATA3(LCDIF,lcdif_data,3)	D10	PWR_PERI02_OUT	yes	gpio3_IO8(GPIO3,gpio_io,8)
81	GND	GND				
82	LCD	lcdif_DATA4(LCDIF,lcdif_data,4)	C10	PWR_PERI02_OUT	yes	gpio3_IO9(GPIO3,gpio_io,9)
83	LCD	lcdif_DATA5(LCDIF,lcdif_data,5)	B10	PWR_PERI02_OUT	yes	gpio3_IO10(GPIO3,gpio_io,10)
84	LCD	lcdif_DATA6(LCDIF,lcdif_data,6)	A10	PWR_PERI02_OUT	yes	gpio3_IO11(GPIO3,gpio_io,11)
85	LCD	lcdif_DATA7(LCDIF,lcdif_data,7)	D11	PWR_PERI02_OUT	yes	gpio3_IO12(GPIO3,gpio_io,12)
86	LCD	lcdif_DATA8(LCDIF,lcdif_data,8)	B11	PWR_PERI02_OUT	yes	gpio3_IO13(GPIO3,gpio_io,13)
87	GND	GND				
88	LCD	lcdif_DATA9(LCDIF,lcdif_data,9)	A11	PWR_PERI02_OUT	yes	gpio3_IO14(GPIO3,gpio_io,14)
89	LCD	lcdif_DATA10(LCDIF,lcdif_data,10)	E12	PWR_PERI02_OUT	yes	gpio3_IO15(GPIO3,gpio_io,15)
90	LCD	lcdif_DATA11(LCDIF,lcdif_data,11)	D12	PWR_PERI02_OUT	yes	gpio3_IO16(GPIO3,gpio_io,16)
91	LCD	lcdif_DATA12(LCDIF,lcdif_data,12)	C12	PWR_PERI02_OUT	yes	gpio3_IO17(GPIO3,gpio_io,17)
92	LCD	lcdif_DATA13(LCDIF,lcdif_data,13)	B12	PWR_PERI02_OUT	yes	gpio3_IO18(GPIO3,gpio_io,18)
93	GND	GND				
94	LCD	lcdif_DATA14(LCDIF,lcdif_data,14)	A12	PWR_PERI02_OUT	yes	gpio3_IO19(GPIO3,gpio_io,19)
95	LCD	lcdif_DATA15(LCDIF,lcdif_data,15)	D13	PWR_PERI02_OUT	yes	gpio3_IO20(GPIO3,gpio_io,20)
96	LCD	lcdif_DATA16(LCDIF,lcdif_data,16)	C13	PWR_PERI02_OUT	yes	gpio3_IO21(GPIO3,gpio_io,21)
97	LCD	lcdif_DATA17(LCDIF,lcdif_data,17)	B13	PWR_PERI02_OUT	yes	gpio3_IO22(GPIO3,gpio_io,22)
98	LCD	lcdif_DATA18(LCDIF,lcdif_data,18)	A13	PWR_PERI02_OUT	yes	gpio3_IO23(GPIO3,gpio_io,23)
99	GND	GND				
100	LCD	lcdif_DATA19(LCDIF,lcdif_data,19)	D14	PWR_PERI02_OUT	yes	gpio3_IO24(GPIO3,gpio_io,24)
101	LCD	lcdif_DATA20(LCDIF,lcdif_data,20)	C14	PWR_PERI02_OUT	yes	gpio3_IO25(GPIO3,gpio_io,25)
102	LCD	lcdif_DATA21(LCDIF,lcdif_data,21)	B14	PWR_PERI02_OUT	yes	gpio3_IO26(GPIO3,gpio_io,26)
103	LCD	lcdif_DATA22(LCDIF,lcdif_data,22)	A14	PWR_PERI02_OUT	yes	gpio3_IO27(GPIO3,gpio_io,27)
104	LCD	lcdif_DATA23(LCDIF,lcdif_data,23)	B16	PWR_PERI02_OUT	yes	gpio3_IO28(GPIO3,gpio_io,28)
105	GND	GND				

106	LCD	lcdif_ENABLE(LCDIF,lcdif_enable)	B8	PWR_PERI02_OUT	yes	gpio3_IO1(GPIO3,gpio_io,1)
107	LCD	lcdif_HSYNC(LCDIF,lcdif_hsync)	D9	PWR_PERI02_OUT	yes	gpio3_IO2(GPIO3,gpio_io,2)
108	LCD	lcdif_RESET(LCDIF,lcdif_reset)	E9	PWR_PERI02_OUT	yes	gpio3_IO4(GPIO3,gpio_io,4)
109	LCD	lcdif_VSYNC(LCDIF,lcdif_vsync)	C9	PWR_PERI02_OUT	yes	gpio3_IO3(GPIO3,gpio_io,3)
110	GND	GND				
111	SDIO	usdhc1_CLK(uSDHC1,usdhc_clk)	C1	PWR_SDIO_OUT	yes	gpio2_IO17(GPIO2,gpio_io,17)
112	SDIO	usdhc1_CMD(uSDHC1,usdhc_cmd)	C2	PWR_SDIO_OUT	yes	gpio2_IO16(GPIO2,gpio_io,16)
113	SDIO	usdhc1_DATA0(uSDHC1,usdhc_data,0)	B3	PWR_SDIO_OUT	yes	gpio2_IO18(GPIO2,gpio_io,18)
114	SDIO	usdhc1_DATA1(uSDHC1,usdhc_data,1)	B2	PWR_SDIO_OUT	yes	gpio2_IO19(GPIO2,gpio_io,19)
115	SDIO	usdhc1_DATA2(uSDHC1,usdhc_data,2)	B1	PWR_SDIO_OUT	yes	gpio2_IO20(GPIO2,gpio_io,20)
116	SDIO	usdhc1_DATA3(uSDHC1,usdhc_data,3)	A2	PWR_SDIO_OUT	yes	gpio2_IO21(GPIO2,gpio_io,21)
117	SDIO	usdhc1_CD_B(uSDHC1,usdhc_cd_b)	J14	PWR_PERI01_OUT	yes	gpio1_IO19(GPIO1,gpio_io,19)
118	GND	GND				
119	UART1	uart1_RX(UART1,uart_tx)	K16	PWR_PERI01_OUT	yes	gpio1_IO17(GPIO1,gpio_io,17)
120	UART1	uart1_TX(UART1,uart_rx)	K14	PWR_PERI01_OUT	yes	gpio1_IO16(GPIO1,gpio_io,16)
121	UART2	uart2_RX(UART2,uart_tx)	J16	PWR_PERI01_OUT	yes	gpio1_IO21(GPIO1,gpio_io,21)
122	UART2	uart2_TX(UART2,uart_rx)	J17	PWR_PERI01_OUT	yes	gpio1_IO20(GPIO1,gpio_io,20)
123	UART3	uart3_RX(UART3,uart_rx)	H16	PWR_PERI01_OUT	yes	gpio1_IO25(GPIO1,gpio_io,25)
124	UART3	uart3_TX(UART3,uart_tx)	H17	PWR_PERI01_OUT	yes	gpio1_IO24(GPIO1,gpio_io,24)
125	GND	GND				
126	UART4	uart4_RX(UART4,uart_tx)	G16	PWR_PERI01_OUT	yes	gpio1_IO29(GPIO1,gpio_io,29)
127	UART4	uart4_TX(UART4,uart_rx)	G17	PWR_PERI01_OUT	yes	gpio1_IO28(GPIO1,gpio_io,28)
128	UART5	uart5_RTS_B(UART5,uart_cts_b)	N17	PWR_PERI01_OUT	yes	gpio1_IO8(GPIO1,gpio_io,8)
129	UART5	uart5_CTS_B(UART5,uart_rts_b)	M15	PWR_PERI01_OUT	yes	gpio1_IO9(GPIO1,gpio_io,9)
130	UART5	uart5_RX(UART5,uart_tx)	G13	PWR_PERI01_OUT	yes	gpio1_IO31(GPIO1,gpio_io,31)
131	UART5	uart5_TX(UART5,uart_rx)	F17	PWR_PERI01_OUT	yes	gpio1_IO30(GPIO1,gpio_io,30)
132	UART6	uart6_TX(UART6,uart_rx)	F5	PWR_PERI01_OUT	yes	gpio4_IO17(GPIO4,gpio_io,17)
133	UART6	uart6_RX(UART6,uart_tx)	E5	PWR_PERI01_OUT	yes	gpio4_IO18(GPIO4,gpio_io,18)
134	GND	GND				
135	USB1	usb_OTG1_ID(USB,usb_otg1_id)	K13	PWR_PERI01_OUT	yes	gpio1_IO0(GPIO1,gpio_io,0)
136	USB1	usb_OTG1_OC(USB,usb_otg1_oc)	L15	PWR_PERI01_OUT	yes	gpio1_IO1(GPIO1,gpio_io,1)
137	USB1	usb_OTG1_PWR(USB,usb_otg1_pwr)	M16	PWR_PERI01_OUT	yes	gpio1_IO4(GPIO1,gpio_io,4)
138	USB1	usb_OTG1_dn	T15	PWR_DCDC5V_OUT		
139	USB1	usb_OTG1_dp	U15	PWR_DCDC5V_OUT		
140	USB1	usb_OTG1_vbus	T12	PWR_DCDC5V_OUT		
141	GND	GND				
142	USB2	usb_OTG2_dn	T13	PWR_DCDC5V_OUT		
143	USB2	usb_OTG3_dp	U13	PWR_DCDC5V_OUT		
144	ENET1	ENET1_TX+		PWR_PERI01_OUT		
145	ENET1	ENET1_TX-		PWR_PERI01_OUT		
146	ENET1	ENET1_RX+		PWR_PERI01_OUT		
147	ENET1	ENET1_RX-		PWR_PERI01_OUT		
148	ENET1	ENET1_LED_A		PWR_PERI01_OUT		
149	ENET1	ENET1_LED_L		PWR_PERI01_OUT		
150	GND	GND				

Module Dimentions



Shielding

Possibility to have a Metal Shielding have to be considered to reduce the EMI Interferences. In many Application Board there is the possibility to have WIFI and GPRS module with Internal Antennas. The Metal Shielding will help to improve the performance of the antenna for the Radio devices.

Since in mass production the module will be placed using Pick&Place machines the Metal Shield will be used by machine to Pick Up the module.

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