ARI

3,5” SMARC i.MX8M PLUS SBC Rev 2.0

Hardware Manual

Revision History:

Doc. Version	MINA Version	Date	Change
V1.0	REV2	2024-04-16	Initial Version

Table of Contents

Introduction

1.1 The SMARC Form factor

The SMARC (“Smart Mobility ARChitecture”) is a versatile small form factor computer on Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented X86 devices and other RISC CPUs may be used as well. The Module power envelope is typically under 6W.

Two Module sizes are defined: 82 mm x 50 mm and 82 mm x 80 mm.

The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5 mm pitch right angle connector (the connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

SMARC module and carrier specifications are available online at: https://www.sget.org/standards/smarc.html

STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

2 Specifications

MAS Elettronica’s SMARC 2.11 carrier is an 3,5” SMARC carrier board ideal for HMI/IoT applications as users can take advantage of the integrated on-board wireless capabilities found on the SMARC 2.11 modules. The carrier has USB 2.0, 2x MIPI CSI-2 camera interfaces, LVDS and DSI outputs, and expansion via two miniPCIe Full size slots. Connect Tech’s SMARC 2.11 carrier board supports the latest generation of ARM SOMs. SMARC 2.11 supports an extended temperature range of -40°C to +85°C.

2.1 Features

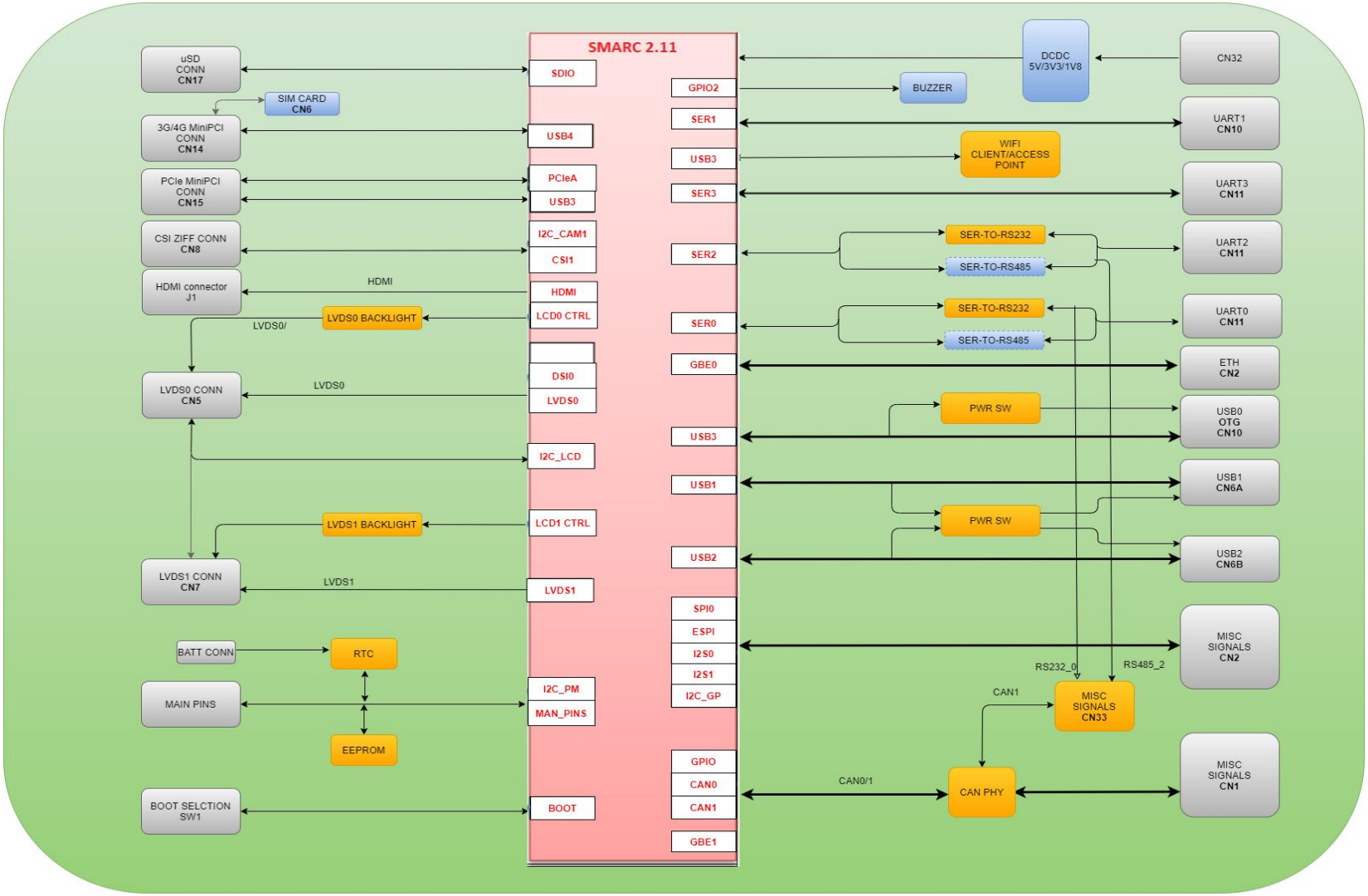
Specifications	
Compatibility	SMARC 2.11
Network	1x RJ-45 GbE
Display	2xLVDS;1xDSI;1xePD
USB	2xUSB2.0 Host; 1x USB OTG
Storage	1xuSD
UART Type	2xRS485;2xRS232;1xTTL
I2C	2xI2C @ 3.3V I/O
GPIO	Min 6 MAX 40 @ 1.8V I/O
SPI	1x SPI 1 bit; 1x SPI 4 bit @ 1.8V I/O
CAN	2x CAN 2.0 (CAN PHY integrated)
EEPROM	1xEEPROM on board
AUDIO	2xI2S channels @ 1.8V I/O
Video Input	1x MIPI CSI-2 (x4 lane)
Expansion	1x miniPCIe Short or full Size slot 1x miniPCIe Short or full Size slot USB for 3G/4G; SIM Card connector
RTC	1x RTC With Battery
LED’s	POWER;USER IO/4G_LED/PCIe_LED/WiFi_LED
Input Power	+9-36V DC Input Power

Specifications	
Dimensions	102 x 146 mm
Operating Temperature	-40°C to +85°C (-40°F to +185°F)

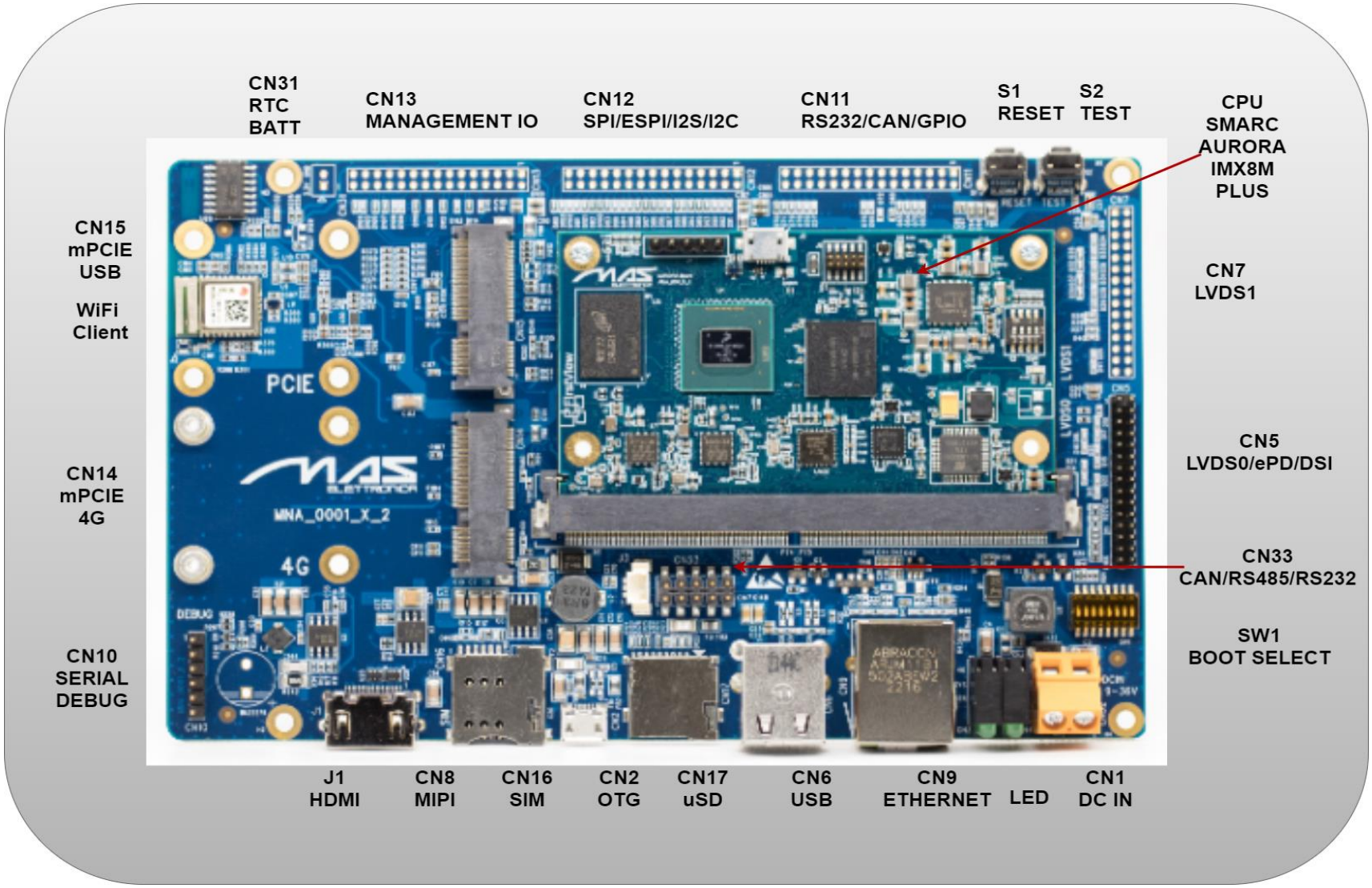
2.2 Part Numbers / Ordering Information

Part Number	
MNA_000_0_1	Complete Mina Carrier Board

2.3 Bock Diagram



2.3 Connector Locations

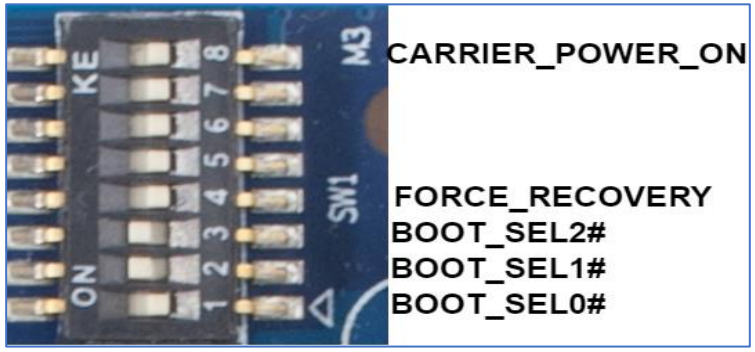


2.3 Boot Modes SW1

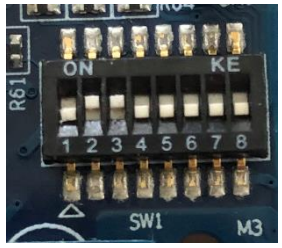
Three BOOT SEL pins allow the Carrier board user to select from eight possible boot devices. Three are Module devices, and four are Carrier devices, and one is a remote device. Below the table from the Hardware specifications 2.0 of the boot modes:

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI (CS0#)
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

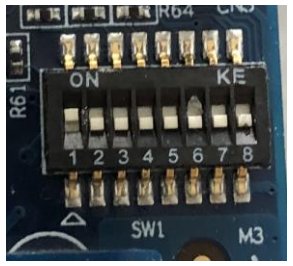
Figure 1 BOOT SEL Selection



BOOT FROM uSD



BOOT FROM eMMC



2.8 Power Supply Voltage

9 V – 36 V

2.9 Mechanical and Environmental

Form Factor

SGET SMARC Specifications v2.0/2.1 (2.1 is currently under approval by SGET)

Dimension

SMARC small size module, 102 x 146 mm

Operating Temperature

Standard: 0°C to +70°C

Rugged: -40°C to +85°C (optional)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

4.0 Pinout and Signal Descriptions

4.1 Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with mandatory PU (pull up) on module
OD	Open drain
I/O	Bi-directional Input/Output
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module
VDD_IN	Main power source from carrier to module
CMOS	Logic input or output
GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	Low Voltage Differential Signal for DisplayPort interface
LVDS D-PHY	Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays
LVDS M-PHY	Low Voltage Differential Signal for MIPI CSI-3 cameras
LVDS LCD	Low Voltage Differential Signal for LCD displays
LVDS PCIE	Low Voltage Differential Signal for PCIe
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
3.3V	3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)

4.2 Network Connector CN9

The carrier provides one 10/100/1000 Ethernet interface

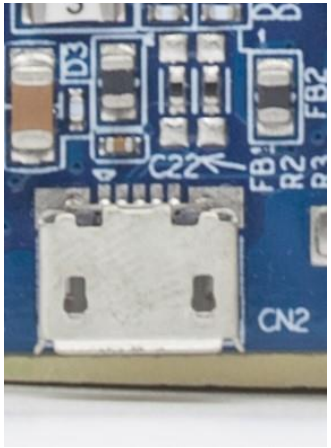
Function	**RJ45 gigabit connector interface**	
Refdes	**CN9**	
Type	LPJG0801FBNL/93626-3006	
Manufacturer	**LINK-PP/Molex**	
Pinout	**Refer to IEEE 802.3 Specification**	

4.3 USB Connector CN6

The carrier provides two USB 2.0 interfaces

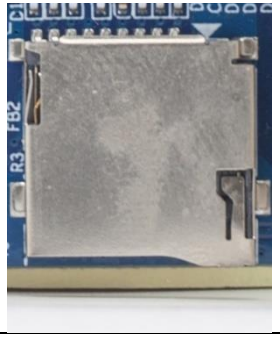
Function	**USB 2.0 connector interface**	
Refdes	**CN6**	
Type	45330890/67298-3090	
Manufacturer	**XIMEY/Molex**	
Pinout	**Refer to Universal Serial Bus 2.0 Specification**	

The carrier provides one USB 2.0 OTG interface

Function	**USB 2.0 OTG connector interface**	
Refdes	**CN2**	
Type	10103594-0001LF	
Manufacturer	**FCI**	
Pinout	**Refer to Universal Serial Bus 2.0 Specification**	

4.4 Micro SD Connector CN17

The carrier provides one micro SD interface

Function	**Micro SD connector interface**	
Refdes	**CN17**	
Type	MCTF-0403	
Manufacturer	**JXT**	
Pinout	**Refer to the** SD Association (sdcard.org)	

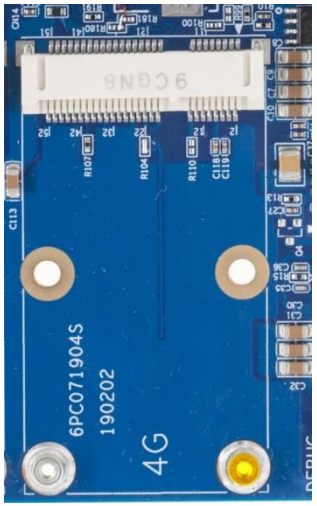
4.5 mPCIe Connector CN14

The carrier provides one miniPCIe 4G Connector

Function	**MiniPCIe connector interface**
Refdes	**CN14**
Type	1775862-2
Manufacturer	**TE**

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	WAKE#	Wake up (GPIO5_3V3)	O	3.3V	P113
2	3.3V_1	3.3V power supply	P	3.3V	
3	NC	Not connected			
4	GND	Digital ground		GND	
5	NC	Not connected			
6	NC	Not connected			
7	NC	Not connected			
8	UIM_PWR	SIM card power supply	P	3.3V	
9	GND	Digital ground		GND	
10	UIM_DATA	SIM card data	I/O	3.3V	
11	NC	Not connected			
12	UIM_CLK	SIM card clock	O	3.3V	
13	NC	Not connected			
14	UIM_RESET	SIM card reset	O	3.3V	
15	GND	Digital ground		GND	
16	UIM_VPP	SIM card power supply	P	3.3V	



17	NC	Not connected			
18	GND	Digital ground		GND	
19	NC	Not connected			
20	NC	NC			
21	GND	Digital ground		GND	
22	4G_RESET#	Functional reset to the card (GPIO4_3V3)	I	3.3V	P112
23	NC	Not connected			
24	3.3VAUX	3.3V power supply	P	3.3V	
25	NC	Not connected			
26	GND	Digital ground		GND	
27	GND	Digital ground		GND	
28	NC	Not connected			
29	GND	Digital ground		GND	
30	NC	Not connected			
31	NC	Not connected			
32	NC	Not connected			
33	NC	Not connected			
34	GND	Digital ground		GND	
35	GND	Digital ground		GND	
36	USB_D-	Negative differential USB signal (USB4_N)	I/O		S36
37	GND	Digital ground		GND	
38	USB_D+	Positive differential USB signal (USB4_P)	I/O		S35
39	3.3VAUX	3.3V power supply	P	3.3V	

	40	GND	Digital ground		GND	
	41	3.3VAUX	3.3V power supply	P	3.3V	
	42	LED_WWAN#	WWAN LED status signal	O	3.3V	
	43	GND	Digital ground		GND	
	44	NC	Not connected			
	45	NC	Not connected			
	46	NC	Not connected			
	47	NC	Not connected			
	48	NC	Not connected			
	49	NC	Not connected			
	50	GND	Digital ground		GND	
	51	NC	Not connected			
	52	3.3V	3.3V power supply	P	3.3V	

4.6 mPCIe Connector CN15

The carrier provides one miniPCie WiFi Connector

Function	**MiniPCIe connector interface**	
Refdes	**CN15**	
Type	1775862-2	
Manufacturer	**TE**	

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	WAKE#	Wake up (PCIE_WAKE_3V3)	O	3.3V	S146
2	3.3V_1	3.3V power supply	P	3.3V	
3	NC	Not connected			
4	GND	Digital ground		GND	
5	NC	Not connected			
6	1.5V	1.5V power supply	P	1.5V	
7	NC	Not connected			
8	NC	Not connected			
9	GND	Digital ground		GND	
10	NC	Not connected			
11	REFCLK-	Negative differential reference clock (PCIE_REFCLK_DN) PCIe REF clock Negative	IN	PCIe	
12	NC	Not connected			
13	REFCLK+	Positive differential reference clock (PCIE_REFCLK_DP) PCIe REF clock Positive	IN	PCIe	
14	NC	Not connected			
15	GND	Digital ground		GND	
16	NC	Not connected			
17	RESERVED	Reserved			
18	GND	Digital ground		GND	
19	RESERVED	Reserved			
20	W_DISABLE	WLAN disable (GPIO6_3V3)	O	3.3V	P114
21	GND	Digital ground		GND	

22	PERST#	Functional reset to the card (PCIE_A_RST_3V3)	I	3.3V	P75
23	PERN0	Negative differential receive signal (PCIE_A_RX_N)	I		P87
24	3.3VAUX	3.3V power supply	P	3.3V	
25	PERP0	Positive differential receive signal (PCIE_A_RX_P)	I		P86
26	GND	Digital ground		GND	
27	GND	Digital ground		GND	
28	1.5V	1.5V power supply	P	1.5V	
29	GND	Digital ground		GND	
30	NC	Not connected			
31	PETN0	Negative differential transmit signal (PCIE_A_TX_I_N)	O	PCIe	P90
32	NC	Not connected			
33	PETP0	Positive differential transmit signal (PCIE_A_TX_I_P)	O	PCIe	P89
34	GND	Digital ground		GND	
35	GND	Digital ground		GND	
36	USB_D-	Negative differential USB signal (USB3_N)	I/O		S69
37	GND	Digital ground		GND	
38	USB_D+	Positive differential USB signal (USB3_P)	I/O		S68
39	3.3VAUX	3.3V power supply	P	3.3V	
40	GND	Digital ground		GND	
41	3.3VAUX	3.3V power supply	P	3.3V	

	42	LED_WWAN#	WWAN LED status signal	O	3.3V	
	43	GND	Digital ground		GND	
	44	LED_WLAN#	WLAN LED status signal	O	3.3V	
	45	RESERVED	Reserved			
	46	NC	Not connected			
	47	RESERVED	Reserved			
	48	1.5V	1.5V power supply	P	1.5V	
	49	RESERVED	Reserved			
	50	GND	Digital ground		GND	
	51	RESERVED	Reserved			
	52	3.3V	3.3V power supply	P	3.3V	

4.7 Serial Debug Connector CN10

The carrier provides one micro SD interface

Function	**Serial Debug 3V3 TTL connector interface**	
Refdes	**CN10**	
Type	WB250SV-06STD03	
Manufacturer	**JXT**	

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	GND	Digital ground		GND	
4	UART RX	UART RX INPUT SIGNAL (SER1_RX)	I/O	3.3V	P135
5	UART TX	UART TX OUTPUT SIGNAL (SER1_TX)	I/O	3.3V	P134
2,3,6	NC	Not connected	-	-	

4.8 DC IN Connector CN1

The carrier Power input 9-36V

Function	**Input power 9-36V**
Refdes	**CN1**
Type	DG127-5.08-02P-14-02A(H)
Manufacturer	**DEGSON**

Pinout

Pin	Signal name	Description	I/O	Power rail	Note
1	DC IN	Power input inverse polarity protected	P	9-36V	
2	GND	Ground signal	P	GND	

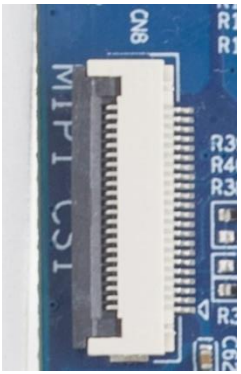
4.8 MIPI CSI2 IN Connector CN8

The carrier provides a 22 pin CSI2 input connector

Function	CSI2 input connector
Refdes	**CN8**
Type	687122149022
Manufacturer	**Wurth**

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	3V3	3V3 Power supply	P	3V3	
2	SDA	SDA I2C 3V3 SIGNAL (I2C_CAM1_DAT_3V3)	I/O	3V3	S2
3	SCL	SCL I2C 3V3 SIGNAL (i2C_CAM1_CK_3V3)	I/O	3V3	S1
4	GND	Ground signal	P	GND	
5	MCLK	Sensor reference clock	I/O	3V3	S6
6	Power Down	Sensor power down (GPIO1)	I/O	3V3	P109
7	GND	Ground signal	P	GND	



	8	CSI_D3_P	Sensor Data 3 positive	IN	MIPI	P16
	9	CSI_D3_N	Sensor Data 3 negative	IN	MIPI	P17
	10	GND	Ground signal	P	GND	
	11	CSI_D2_P	Sensor Data 2 positive	IN	MIPI	P13
	12	CSI_D2_N	Sensor Data 2 negative	IN	MIPI	P14
	13	GND	Ground signal	P	GND	
	14	CSI_CK_P	Sensor CLOCK positive	IN	MIPI	P3
	15	CSI_CK_N	Sensor CLOCK negative	IN	MIPI	P4
	16	GND	Ground signal	P	GND	
	17	CSI_D1_P	Sensor Data 1 positive	IN	MIPI	P10
	18	CSI_D1_N	Sensor Data 1 negative	IN	MIPI	P11
	19	GND	Ground signal	P	GND	
	20	CSI_D0_P	Sensor Data 0 positive	IN	MIPI	P7
	21	CSI_D0_N	Sensor Data 0 negative	IN	MIPI	P8
	22	GND	Ground signal	P	GND	

4.9 RTC Batt Connector CN31

The 3V Battery in Connector

Function	**RTC Batt 3V**
Refdes	**CN31**
Type	Strip 1x2 P=2mm
Manufacturer	**SAMTEC**
Pinout	

Pin	Signal name	Description	I/O	Power rail	Note
1	VBATT IN	Battery Input for RTC	P	3V	
2	GND	Ground signal	P	GND	

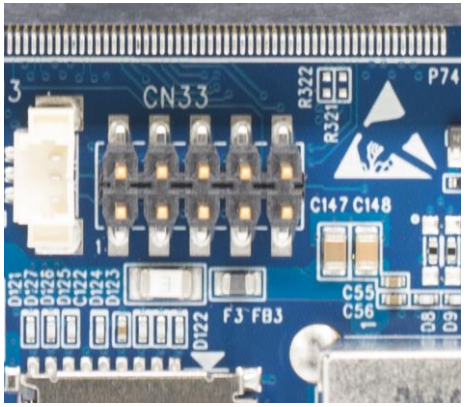
4.10 CN33 Serial/CAN connector

The carrier Power input 9-36V

Function	**Serial CAN Connector**
Refdes	**CN33**
Type	STRIP 2X5 passo 2,54mm
Manufacturer	**SAMTEC**

Pinout

Pin	Signal name	Description	I/O	Power rail	Note
1	SERIAL_0_RS232_TX	RS232 TX SIGNAL	I/O	3V3	
2	SERIAL_0_RS232_RTS	RS232 RTS SIGNAL	I/O	RS232	
3	SERIAL_0_RS232_RX	RS232 RX SIGNAL	I/O	RS232	
4	SERIAL_0_RS232_CTS	RS232 CTS SIGNAL	I/O	RS232	
5	RS485_B2	RS485 B2 SIGNAL	I/O	RS485	
6	RS485_A2	RS485 A2 SIGNAL	I/O	RS485	
7	CAN1_L	CAN1 L SIGNAL	I/O	CAN	
8	CAN1_H	CAN1 H SIGNAL	I/O	CAN	
9	GND	Ground signal	P		
10	GND	Ground signal	P		



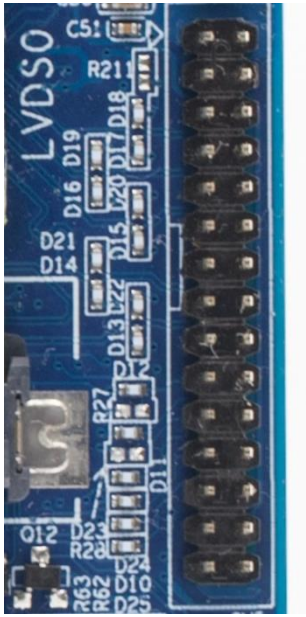
4.11 LVDS0/ePD/DSI Connector CN5

The carrier provides a 30 pin LVDS0/ePD/DSI connector

Function	LVDS0/ePD/DSI connector
Refdes	**CN5**
Type	TMMH-115-01-T-D (2x15 P=2mm)
Manufacturer	**SAMTEC**

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	3V3	3V3 Power supply	P	3V3	
2	3V3	3V3 Power supply	P	3V3	
3	DP0_HPD	ePD Hot Plug signal	I/O	1V8	S113
4	5V	5V Power supply	P	5V	
5	GND	Ground signal	P	GND	
6	GND	Ground signal	P	GND	
7	LVDS_DSI_0_0_N	LVDS CHANNEL 0 NEGATIVE SIGNAL	OUT	LVDS	S126
8	LVDS_DSI_0_0_P	LVDS CHANNEL 0 POSITIVE SIGNAL	OUT	LVDS	S125
9	LVDS_DSI_0_1_N	LVDS CHANNEL 1 NEGATIVE SIGNAL	OUT	LVDS	S129
10	LVDS_DSI_0_1_P	LVDS CHANNEL 1 POSITIVE SIGNAL	OUT	LVDS	S128
11	LVDS_DSI_0_2_N	LVDS CHANNEL 0 DATA 2 NEGATIVE SIGNAL	OUT	LVDS	S132
12	LVDS_DSI_0_2_P	LVDS CHANNEL 0 DATA 2 POSITIVE SIGNAL	OUT	LVDS	S131
13	GND	Ground signal	P	GND	



	14	GND	Ground signal	P	GND	
	15	LVDS_DSI_0_CK_N	LVDS CHANNEL 0 CLOCK NEGATIVE SIGNAL	OUT	LVDS	S135
	16	LVDS_DSI_0_CK_P	LVDS CHANNEL 0 CLOCK POSITIVE SIGNAL	OUT	LVDS	S134
	17	LVDS_DSI_0_3_N	LVDS CHANNEL 3 NEGATIVE SIGNAL	OUT	LVDS	S138
	18	LVDS_DSI_0_3_P	LVDS CHANNEL 3 POSITIVE SIGNAL	OUT	LVDS	S137
	19	I2C_LCD0_DAT_3V3	I2C DATA FOR DISPLAY	I/O	3V3	S140
	20	I2C_LCD0_CLK_3V3	I2C CLOCK FOR DISPLAY	I/O	3V3	S139
	21	GPIO8_3V3	GPIO FOR TOUCH RESET	OUT	3V3	P116
	22	INT0	GPIO FOR TOUCH INTERRUPT	IN	3V3	P119
	23	LCD0_BKLT_PWM	PWM FOR BACKLIGHT CONTROL	OUT	3V3	S141
	24	LCD0_BKLT_EN	PWM FOR BACKLIGHT ENABLE	OUT	3V3	S127
	25	NC	Non connesso			
	26	VSYSTEM	9-36V power from main power supply	P	9-36V	
	27	LED0-	BACKLIGHT LED0 – POWER SUPPLY	P		
	28	LED0-	BACKLIGHT LED0 + POWER SUPPLY	P		
	29	LED0-	BACKLIGHT LED0 – POWER SUPPLY	P		
	30	LED0-	BACKLIGHT LED0 + POWER SUPPLY	P		

4.12 LVDS1 Connector CN7

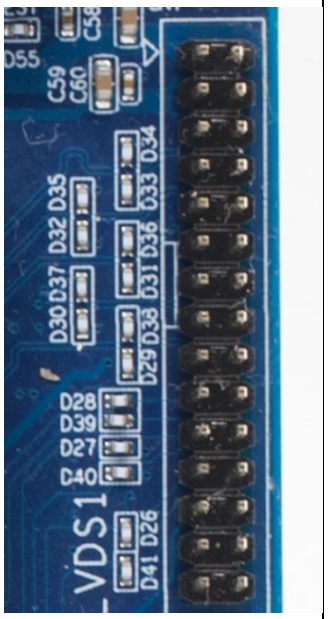
The carrier provides a 30 pin LVDS1 connector

Function	LVDS1 connector	

Refdes	**CN7**
Type	TMMH-115-01-T-D (2x15 P=2mm)
Manufacturer	**SAMTEC**

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	3V3	3V3 Power supply	P	3V3	
2	3V3	3V3 Power supply	P	3V3	
3	DP0_HPD	ePD Hot Plug signal	I/O	3V3	S113
4	5V	5V Power supply	P	5V	
5	GND	Ground signal	P	GND	
6	GND	Ground signal	P	GND	
7	LVDS _1_0_N	LVDS CHANNEL 1 DATA 0 NEGATIVE SIGNAL	OUT	LVDS	S112
8	LVDS_1_0_P	LVDS CHANNEL 1 DATA 0 POSITIVE SIGNAL	OUT	LVDS	S111
9	LVDS_1_1_N	LVDS CHANNEL 1 DATA 1 NEGATIVE SIGNAL	OUT	LVDS	S115
10	LVDS_1_1_P	LVDS CHANNEL 1 DATA 1 POSITIVE SIGNAL	OUT	LVDS	S114
11	LVDS_1_2_N	LVDS CHANNEL 1 DATA 2 NEGATIVE SIGNAL	OUT	LVDS	S118
12	LVDS_1_2_P	LVDS CHANNEL 1 DATA 2 POSITIVE SIGNAL	OUT	LVDS	S117
13	GND	Ground signal	P	GND	
14	GND	Ground signal	P	GND	
15	LVDS_1_CK_N	LVDS CHANNEL 1 CLOCK NEGATIVE SIGNAL	OUT	LVDS	S109
16	LVDS_1_CK_P	LVDS CHANNEL 1 CLOCK POSITIVE SIGNAL	OUT	LVDS	S108
17	LVDS_1_3_N	LVDS CHANNEL 1 DATA 3 NEGATIVE SIGNAL	OUT	LVDS	S121
18	LVDS_1_3_P	LVDS CHANNEL 1 DATA 3 POSITIVE SIGNAL	OUT	LVDS	S120



19	LCD_I2C_DATA	I2C DATA FOR DISPLAY	I/O	3V3	S140	
20	LCD_I2C_CLOCK	I2C CLOCK FOR DISPLAY	I/O	3V3	S139	
21	GPIO10_3V3	GPIO FOR TOUCH RESET	OUT	3V3	P118	
22	INT1	GPIO FOR TOUCH INTERRUPT (GPIO11)	IN	3V3	P119	
23	LCD1_BKLT_PWM	PWM FOR BACKLIGHT CONTROL	OUT	3V3	S122	
24	LCD1_BKLT_EN	PWM FOR BACKLIGHT ENABLE	OUT	3V3	S107	
25	NC	Non connesso				
26	VSYSTEM	9-36V power from main power supply	P	9-36V		
27	LED1-	BACKLIGHT LED1– POWER SUPPLY	P			
28	LED1-	BACKLIGHT LED1 + POWER SUPPLY	P			
29	LED1-	BACKLIGHT LED1 – POWER SUPPLY	P			
30	LED1-	BACKLIGHT LED1 + POWER SUPPLY	P			

4.13 RS232/CAN/GPIO CN11

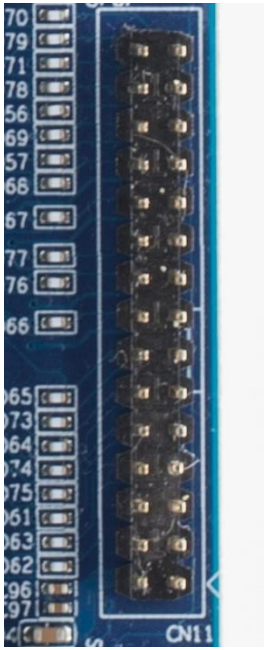
The carrier provides a 30 pin RS232/CAN/GPIO connector

Function	RS232/CAN/GPIO connector
Refdes	**CN11**
Type	TMMH-115-01-T-D (2x15 P=2mm)
Manufacturer	**SAMTEC**

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	3V3	3V3 Power supply	P	3V3	

2	3V3	3V3 Power supply	P	3V3	
3	3V3	3V3 Power supply	P	3V3	
4	GND	Ground signal	P	GND	
5	GND	Ground signal	P	GND	
6	GND	Ground signal	P	GND	
7	TXD0	RS232TX SIGNAL FROM UART 0	OUT	RS232	P129
8	GPIO2	GPIO2 SIGNAL FROM SOM	IN/OUT	3V3	P110
9	RXD0	RS232 RX SIGNAL FROM UART 0	IN	RS232	P130
10	GPIO3	GPIO3 SIGNAL FROM SOM	IN/OUT	3V3	P111
11	CTS0	RS232 CTS SIGNAL FROM UART 0	IN/OUT	RS232	P132
12	GPIO4	GPIO2 SIGNAL FROM SOM	IN/OUT	3V3	P112
13	RTS0	RS232 RTS SIGNAL FROM UART 0	IN/OUT	RS232	P131
14	GPIO5	GPIO2 SIGNAL FROM SOM	IN/OUT	3V3	P113
15	RS485_A0	RS485 SER0 POSITIVE SIGNAL	IN/OUT	RS485	
16	GPIO6	GPIO2 SIGNAL FROM SOM	IN/OUT	3V3	P114
17	RS485_B0	RS485 SER0 NEGATIVE SIGNAL	IN/OUT	RS485	
18	GPIO7	GPIO2 SIGNAL FROM SOM	IN/OUT	3V3	P115
19	RS485_A2	RS485 SER2 POSITIVE SIGNAL	IN/OUT	RS485	
20	CAN0_TX	CAN0 TX SIGNAL FROM SOM	OUT	3V3	P143
21	RS485_B2	RS485 SER2 NEGATIVE SIGNAL	IN/OUT	RS485	
22	CAN0_RX	CAN0 RX SIGNAL FROM SOM	IN	3V3	P144
23	TXD2	RS232 TX SIGNAL FROM UART 2	OUT	RS232	P136
24	CAN1_TX	CAN1 TX SIGNAL FROM SOM	OUT	3V3	P145



25	RXD2	RS232 RX SIGNAL FROM UART 2	IN	RS232	P135	
26	CAN1_RX	CAN1 RX SIGNAL FROM SOM	IN	3V3	P146	
27	CTS2	RS23 2CTS SIGNAL FROM UART 2	IN/OUT	RS232	P139	
28	UART3_TX	SERIAL 3 TX TTL SIGNAL FROM SOM	OUT	3V3	P140	
29	RTS2	RS232 RTS SIGNAL FROM UART 2	IN/OUT	RS232	P138	
30	UART3_RX	SERIAL 3 RX TTL SIGNAL TO SOM	IN	3V3	P141	

4.14 SPI/ESPI/I2S/I2C CN12

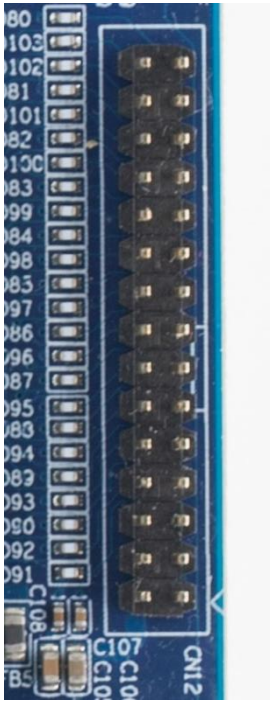
The carrier provides a 30 pin RS232/CAN/GPIO connector

Function	SPI/ESPI/I2S/I2C connector
Refdes	**CN12**
Type	TMMH-115-01-T-D (2x15 P=2mm)
Manufacturer	**SAMTEC**

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	3V3	3V3 Power supply	P	3V3	
2	3V3	3V3 Power supply	P	3V3	
3	3V3	3V3 Power supply	P	3V3	
4	GND	Ground signal	P	GND	
5	GND	Ground signal	P	GND	
6	GND	Ground signal	P	GND	

7	ESPI_ALERT0	ESPI_ALERT0 SIGNAL FROM SOM CAN BE A GPIO	INOUT	1V8	S43
8	I2C_GP_DATA	I2C DATA GP BUS SIGNAL	IN/OUT	1V8	S49
9	ESPI_RESET	ESPI RESET SIGNAL FROM SOM CAN BE A GPIO	OUT	1V8	S58
10	I2C_GP_CLOCK	I2C CLOCK GP BUS SIGNAL	IN/OUT	1V8	S48
11	ESPI_CLK	ESPI CLOCK SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	P56
12	I2S2_CK	I2S2_CK SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S53
13	ESPI_CS0	ESPI_CS0 SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	P54
14	I2S2_LRCK	I2S2_LRCK SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S50
15	ESPI_IO_0	ESPI_IO_0 SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	P57
16	I2S2_SDOUT	2S2_SDOUT SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S51
17	ESPI_IO_1	ESPI_IO_1 SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	P58
18	I2S2_SDIN	I2S2_SDIN SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S52
19	ESPI_IO_2	ESPI_IO_2 SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S56
20	I2S0_SDOUT	I2S0_SDOUT SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	S40
21	ESPI_IO_3	ESPI_IO_3 SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S57
22	I2S0_SDIN	I2S0_SDIN SIGNAL FROM SOM CAN BE GPIO	IN	1V8	S52
23	SPI0_CS0	SPI0_CS0 SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	P43
24	AUDIO_MCK	AUDIO_MCK SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	S38
25	SPI0_CK	SPI0_CK SIGNAL FROM SOM CAN BE GPIO	IN	1V8	P44
26	I2S0_LRCK	I2S0_LRCK SIGNAL FROM SOM CAN BE GPIO	IN	1V8	S39
27	SPI0_DIN	SPI0_DIN SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	P45
28	I2S0_CK	I2S0_CK SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	S42



	29	SPI0_DO	SPI0_DO SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	P46
	30	DP0_HPD	DP0_HPD SIGNAL FROM SOM CAN BE GPIO	IN	1V8	S113

4.15 MANAGEMENT IO CN13

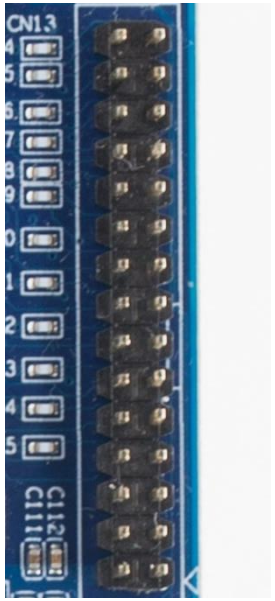
The carrier provides a 30 pin MANAGEMENT IO connector

Function	MANAGEMENT IO connector
Refdes	**CN13**
Type	TMMH-115-01-T-D (2x15 P=2mm)
Manufacturer	**SAMTEC**

Pinout

Pin	Signal name	Description	I/O	Power rail	SMARC CONN PIN
1	3V3	3V3 Power supply	P	3V3	
2	3V3	3V3 Power supply	P	3V3	
3	3V3	3V3 Power supply	P	3V3	
4	GND	Ground signal	P	GND	
5	GND	Ground signal	P	GND	
6	GND	Ground signal	P	GND	
7	I2C_PM_CK	I2C_PM_CK SIGNAL FROM SOM CAN BE A GPIO	INOUT	1V8	P121
8	SD1_CLK	SD1_CLK GP BUS SIGNAL	IN/OUT	1V8	S19
9	I2C_PM_DAT	I2C_PM_DAT SIGNAL FROM SOM CAN BE A GPIO	OUT	1V8	P122
10	SD1_CMD	SD1_CMD BUS SIGNAL CAN BE A GPIO	IN/OUT	1V8	S122

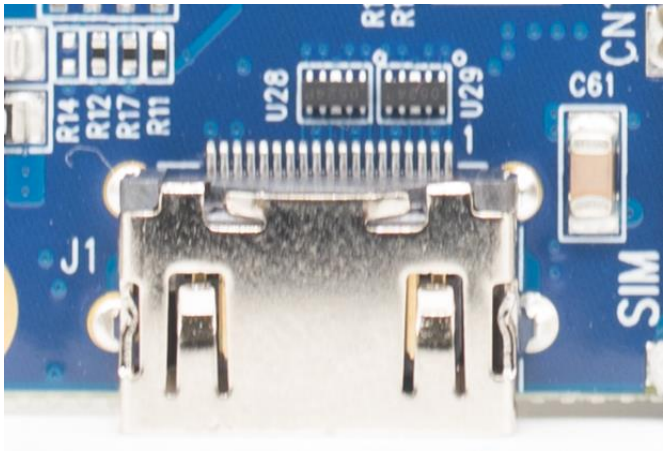
11	SLEEP	SLEEP SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S149
12	SD1_RESET_B	SD1_RESET_B SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S31
13	RESET_OUT	RESET_OUT# FROM SOM	IN/OUT	1V8	P126
14	SD1_STROBE	SD1_STROBE SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S28
15	RESET_IN	RESET_IN# SIGNAL TO SOM	IN/OUT	1V8	P127
16	SD1_DATA0	SD1_DATA0 SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S17
17	POWER_BTN	POWER_BTN# SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	P128
18	SD1_DATA1	SD1_DATA1 SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S18
19	CHARGING	CHARGING SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S151
20	SD1_DATA2	SD1_DATA2 SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	S20
21	CHARGER_PRSNT	CHARGER_PRSNT SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S152
22	SD1_DATA3	SD1_DATA3 SIGNAL FROM SOM CAN BE GPIO	IN	1V8	S21
23	CHARGER_STBY	CHARGER_STBY# SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	S153
24	SD1_DATA4	SD1_DATA4 SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	S23
25	SD2_WP	SD2_WP SIGNAL FROM SOM CAN BE GPIO	IN	1V8	P33
26	SD1_DATA5	SD1_DATA5 SIGNAL FROM SOM CAN BE GPIO	IN	1V8	S24
27	BATLOW	BATLOW# SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S156
28	SD1_DATA6	SD1_DATA6 SIGNAL FROM SOM CAN BE GPIO	OUT	1V8	S26
29	TEST	TEST SIGNAL FROM SOM CAN BE GPIO	IN/OUT	1V8	S157
30	SD1_DATA7	SD1_DATA7 SIGNAL FROM SOM CAN BE GPIO	IN	1V8	S27



4.16 HDMI CONNECTOR J1

The carrier provides a HDMI standard Connector

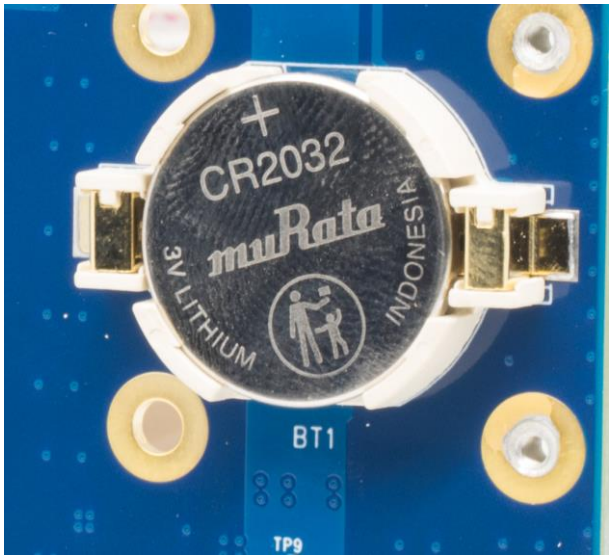
Function	HDMI CONNECTOR
Refdes	**J1**
Type	10029449-111RLF
Manufacturer	**FCI**



4.17 BATTERY CONNECTOR BT1

The carrier provides a BATTERY CR2032

Function	HDMI CONNECTOR
Refdes	**BT1**
Type	BU2032SM-HD-G
Manufacturer	**MPD**



4.2 The SMARC Connector CN18

The SMARC Module pins are designated as P1 – P156 on the Module Primary (Top) side, and S1 – S158 on the Module Secondary (Bottom) side. There is a total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used. Some connector vendors offer "reverse" pin-out connectors, which effectively flip the Module over such that the Module Primary side would face the Carrier board.

The SMARC Module pins are deliberately numbered as P1 – P156 and S1 – S158 for clarity and to differentiate the SMARC Module from MXM3 graphics modules, which use the same connector but use the pins for very different functions. MXM3 cards and MXM3 baseboard connectors use a different pin numbering scheme.

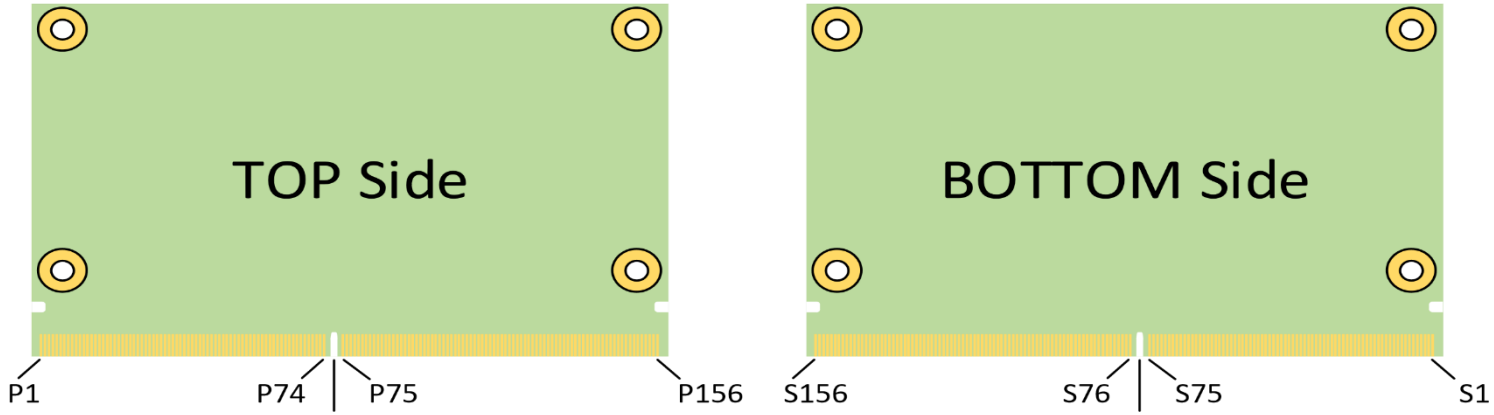
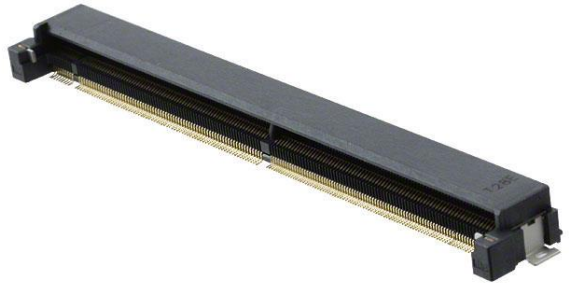


Figure 3 Module top/bottom side pin numbering

The processor and chipset are implemented on the SMARC 2.11 Module, which connects to the MINA SMARC 2.11 Carrier via a MXM 3.0 fine pitch connector:

Function	**SMARC 2.11 Module Interface**	
Refdes	**CN18**	
Type	**JAE Electronics MXM 3.0 Connector**	
Manufacturer	**MM70-314-310B1-2-R300 Manufacturer: JAE Electronics**	
Pinout	**See the paragraph 4.3 for Carrier Pinout. For Standard complete pinout refer to SMARC Hardware Specification V2.0**	

The below table is a comprehensible list of all signal pins on the MXM 3 connector in the standard specification SMARC 2.1.

4.1 Module Pinout Top Side P

P-Pin Primary (Top) Side	
P1	SMB_ALERT_1V8#
P2	GND
P3	CSI1_CK+
P4	CSI1_CK-
P5	GBE1_SDP
P6	GBE0_SDP
P7	CSI1_RX0+
P8	CSI1_RX0-
P9	GND
P10	CSI1_RX1+
P11	CSI1_RX1-
P12	GND
P13	CSI1_RX2+
P14	CSI1_RX2-
P15	GND
P16	CSI1_RX3+
P17	CSI1_RX3-
P18	GND
P19	GBE0_MDI3-
P20	GBE0_MDI3+
P21	GBE0_LINK100#
P22	GBE0_LINK1000#
P23	GBE0_MDI2-
P24	GBE0_MDI2+
P25	GBE0_LINK_ACT#
P26	GBE0_MDI1-
P27	GBE0_MDI1+

P-Pin Primary (Top) Side	
P28	GBE0_CTREF
P29	GBE0_MDI0-
P30	GBE0_MDI0+
P31	SPI0_CS1#
P32	GND
P33	SDIO_WP
P34	SDIO_CMD
P35	SDIO_CD#
P36	SDIO_CK
P37	SDIO_PWR_EN
P38	GND
P39	SDIO_D0
P40	SDIO_D1
P41	SDIO_D2
P42	SDIO_D3
P43	SPI0_CS0#
P44	SPI0_CK
P45	SPI0_DIN
P46	SPI0_DO
P47	GND
P48	~~SATA_TX+~~
P49	~~SATA_TX-~~
P50	GND
P51	~~SATA_RX+~~
P52	~~SATA_RX-~~
P53	GND
P54	ESPI_CS0#
P55	ESPI_CS1#

P-Pin Primary (Top) Side	
P56	ESPI_CK
P57	ESPI_IO_1
P58	ESPI_IO_0
P59	GND
P60	USB0+
P61	USB0-
P62	USB0_EN_OC#
P63	USB0_VBUS_DET
P64	USB0_OTG_ID
P65	USB1+
P66	USB1-
P67	USB1_EN_OC#
P68	GND
P69	USB2+
P70	USB2-
P71	USB2_EN_OC#
P72	RSVD
P73	RSVD
P74	USB3_EN_OC#
	Key
P75	PCIE_A_RST#
P76	USB4_EN_OC#

P-Pin Primary (Top) Side	
P77	RSVD
P78	RSVD
P79	GND
P80	~~PCIE_C_REFCK+~~
P81	~~PCIE_C_REFCK-~~
P82	GND
P83	PCIE_A_REFCK+
P84	PCIE_A_REFCK-
P85	GND
P86	PCIE_A_RX+
P87	PCIE_A_RX-
P88	GND
P89	PCIE_A_TX+
P90	PCIE_A_TX-
P91	GND
P92	HDMI_D2+ / DP1_LANE0+
P93	HDMI_D2- / DP1_LANE0-
P94	GND

P-Pin Primary (Top) Side	
P95	HDMI_D1+ / DP1_LANE1+
P96	HDMI_D1- / DP1_LANE1-
P97	GND
P98	HDMI_D0+ / DP1_LANE2+
P99	HDMI_D0- / DP1_LANE2-
P100	GND
P101	HDMI_CK+ / DP1_LANE3+
P102	HDMI_CK- / DP1_LANE3-
P103	GND
P104	HDMI_HPD / DP1_HPD
P105	HDMI_CTRL_CK / DP1_AUX+
P106	HDMI_CTRL_DAT / DP1_AUX-
P107	~~DP1_AUX_SEL~~
P108	GPIO0

P-Pin Primary (Top) Side	
P109	GPIO1
P110	GPIO2
P111	GPIO3
P112	GPIO4
P113	GPIO5
P114	GPIO6 / ~~TACHIN~~
P-Pin	Primary (Top) Side
P115	GPIO7
P116	GPIO8
P117	GPIO9

P-Pin Primary (Top) Side	
P118	GPIO10
P119	GPIO11
P120	GND
P121	I2C_PM_CK
P122	I2C_PM_DAT
P123	BOOT_SEL0#
P124	BOOT_SEL1#
P125	BOOT_SEL2#
P126	RESET_OUT#
P127	RESET_IN#

P-Pin Primary (Top) Side	
P128	POWER_BTN#
P129	SER0_TX
P130	SER0_RX
P131	SER0_RTS#
P132	SER0_CTS#
P133	GND
P134	SER1_TX
P135	SER1_RX
P136	SER2_TX
P137	SER2_RX

P-Pin Primary (Top) Side	
P138	SER2_RTS#
P139	SER2_CTS#
P140	SER3_TX
P141	SER3_RX
P142	GND
P143	CAN0_TX
P144	CAN0_RX
P145	CAN1_TX
P146	CAN1_RX
P147	VDD_IN

P-Pin Primary (Top) Side	
P148	VDD_IN
P149	VDD_IN
P150	VDD_IN
P151	VDD_IN
P152	VDD_IN
P153	VDD_IN
P154	VDD_IN
P155	VDD_IN
P156	VDD_IN

4.2 Module Pinout Top Side S

SPin Secondary (Bott) Side	
S1	~~CSI1_TX+~~ /
S2	~~CSI1_TX-~~ /
S3	GND
S4	RSVD

SPin Secondary (Bott) Side	
S5	~~CSI0_TX-~~
S6	CAM_MCK
S7	~~CSI0_TX+~~
S8	CSI0_CK+

SPin Secondary (Bott) Side	
S9	CSI0_CK-
S10	GND
S11	CSI0_RX0+
S12	CSI0_RX0-

SPin Secondary (Bott) Side	
S13	GND
S14	CSI0_RX1+
S15	CSI0_RX1-
S16	GND

SPin Secondary (Bott) Side	
S17	GBE1_MDI0+
S18	GBE1_MDI0-
S19	GBE1_LINK100#
S20	GBE1_MDI1+

SPin Secondary (Bott) Side	
S21	GBE1_MDI1-
S22	GBE1_LINK1000#
S23	~~GBE1_MDI2+~~
S24	~~GBE1_MDI2-~~
S25	GND
S26	~~GBE1_MDI3+~~
S27	~~GBE1_MDI3-~~
S28	~~GBE1_CTREF~~
S29	~~PCIE_D_TX+~~
S30	~~PCIE_D_TX-~~
S31	~~GBE1_LINK_ACT#~~
S32	~~PCIE_D_RX+~~
S33	~~PCIE_D_RX-~~
S34	GND
S35	USB4+
S36	USB4-
S37	~~USB3_VBUS_DET~~
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT
S41	I2S0_SDIN
S42	I2S0_CK
S43	ESPI_ALERT0#
S44	ESPI_ALERT1#
S45	MDIO_CLK
S46	MDIO_DAT
S47	GND

SPin Secondary (Bott) Side	
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	I2S2_LRCK
S51	I2S2_SDOUT
S52	I2S2_SDIN
S53	I2S2_CK
S54	~~SATA_ACT#~~
S55	~~USB5_EN_OC#~~
S56	ESPI_IO_2
S57	ESPI_IO_3
S58	ESPI_RESET#
S59	~~USB5+~~
S60	~~USB5-~~
S61	GND
S62	~~USB3_SSTX+~~
S63	~~USB3_SSTX-~~
S64	GND
S65	~~USB3_SSRX+~~
S66	~~USB3_SSRX-~~
S67	GND
S68	USB3+
S69	USB3-
S70	GND
S71	~~USB2_SSTX+~~
S72	~~USB2_SSTX-~~
S73	GND
S74	~~USB2_SSRX+~~

SPin Secondary (Bott) Side	
S75	~~USB2_SSRX-~~
	Key
S76	~~PCIE_B_RST#~~
S77	~~PCIE_C_RST#~~
S78	~~PCIE_C_RX+~~
S79	~~PCIE_C_RX-~~
S80	GND
S-Pin	Secondary (Bottom) Side
S81	~~PCIE_C_TX+ / SERDES_2_TX+~~
S82	~~PCIE_C_TX- / SERDES_2_TX-~~
S83	GND
S84	~~PCIE_B_REFCK+~~
S85	~~PCIE_B_REFCK-~~
S86	GND
S87	~~PCIE_B_RX+~~
S88	~~PCIE_B_RX-~~
S89	GND
S90	~~PCIE_B_TX+~~
S91	~~PCIE_B_TX-~~
S92	GND
S93	~~DP0_LANE0+~~
S94	~~DP0_LANE0-~~
S95	~~DP0_AUX_SEL~~
S96	~~DP0_LANE1+~~
S97	~~DP0_LANE1-~~
S98	~~DP0_HPD~~

SPin Secondary (Bott) Side	
S99	~~DP0_LANE2+~~
S100	~~DP0_LANE2-~~
S101	GND
S102	~~DP0_LANE3+~~
S103	~~DP0_LANE3-~~
S104	~~USB3_OTG_ID~~
S105	~~DP0_AUX+~~
S106	~~DP0_AUX-~~
S107	LCD1_BKLT_EN
S108	LVDS1_CK+
S109	LVDS1_CK-
S110	GND
S111	LVDS1_0+
S112	LVDS1_0-
S113	eDP1_HPD
S114	LVDS1_1+
S115	LVDS1_1-
S-Pin	Secondary (Bottom) Side
S116	LCD1_VDD_EN
S117	LVDS1_2+
S118	LVDS1_2-
S119	GND
S120	LVDS1_3+
S121	LVDS1_3-
S122	LCD1_BKLT_PWM
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-
S133	LCD0_VDD_EN
S134	LVDS0_CK+/eDP0_AUX/ DSI0_CLK+

SPin Secondary (Bott) Side	
S135	LVDS0_CK-/eDP0_AUX- / DSI0_CLK-
S136	GND
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-
S139	I2C_LCD_CK
S140	I2C_LCD_DAT
S141	LCD0_BKLT_PWM
S142	RSVD
S143	GND
S144	~~eDP0_HPD~~ / ~~DSI0_TE~~
S145	~~WDT_TIME_OUT#~~
S146	PCIE_WAKE#
S147	~~VDD_RTC~~
S148	LID#
S149	SLEEP#
S150	VIN_PWR_BAD#
S151	CHARGING#
S152	CHARGER_PRSNT#
S153	CARRIER_STBY#
S154	CARRIER_PWR_ON
S155	FORCE_RECOV#
S156	BATLOW#
S157	TEST#
S158	GND

4.2.1 LVDS0/LVDS1 MODE

In the MINA Board the LVDS0 channel can be sourced from:

1) Smarc Module directly

2) LT8912B DSI to LVDS chip.

The LVDS1 channel can be supplied only from the SMARC Connector.

Below is the table with the Pins used in the smarc connector with the description.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS0_0+ **LVDS0_0-** **LVDS0_1+** **LVDS0_1 -** **LVDS0_2+** **LVDS0_2-** **LVDS0_3+** **LVDS0_3-**	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
LVDS0_CK+ **LVDS0_CK-**	S134 S135	Primary LVDS channel differential pair clock lines	O LVDS LCD		Runtime		
LCD0_VDD_EN	S133	Primary LVDS channel power enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_EN	S127	Primary LVDS channel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_PWM	S141	Primary LVDS channel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS1_0+ **LVDS1_0-** **LVDS1_1+** **LVDS1_1 -** **LVDS1_2+** **LVDS1_2-** **LVDS1_3+** **LVDS1_3-**	S111 S112 S114 S115 S117 S118 S120 S121	Secondary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
LVDS1_CK+ **LVDS1_CK-**	S108 S109	Secondary LVDS channel differential pair clock lines.	O LVDS LCD		Runtime		
LCD1_VDD_EN	S116	Secondary panel power enable, active high	O CMOS	1.8V	Runtime		
LCD1_BKLT_EN	S107	Secondary panel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD1_BKLT_PWM	S122	Secondary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.2.2 DSI MODE (build option)

MAS Elettronica SMARC module has integrated the DSI Bridge as a build option. It drives directly a DSI panel without help of other electronics. The following table shows the pins of the SMARC connector are used when the DSI feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DSI0_D0+ **DSI0_D0-** **DSI0_D1+** **DSI0_D1-** **DSI0_D2+** **DSI0_D2-** **DSI0_D3+** **DSI0_D3-**	S125 S126 S128 S129 S131 S132 S137 S138	Primary DSI panel differential pair data lines	O LVDS D-PHY		Runtime		Build option
DSI0_CLK+ **DSI0_CLK-**	S134 S135	Primary DSI panel differential pair clock lines.	O LVDS D-PHY		Runtime		Build option
LCD0_VDD_EN	S133	Primary panel power enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_EN	S127	Primary panel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_PWM	S141	Primary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
DSI0_TE	S113	Primary DSI panel tearing effect sigal	I CMOS	1.8V	Runtime		
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.2.3 ePD MODE

MAS Elettronica SMARC modules have has integrated the SN65DSI86 DSI to embedded DisplayPort (eDP) bridge. The following table shows the pins of the SMARC connector are used when the ePD feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
eDP0_TX0+ **eDP0_TX0-** **eDP0_TX1+** **eDP0_TX1-** **eDP0_TX2+** **eDP0_TX2-** **eDP0_TX3+** **eDP0_TX3-**	S125 S126 S128 S129 S131 S132 S137 S138	ePD panel differential pair data lines	O LVDS D-PHY		Runtime		Build option
eDP0_AUX+ **eDP0_AUX-**	S134 S135	ePD panel panel differential pair clock lines.	O LVDS D-PHY		Runtime		Build option
LCD0_VDD_EN	S133	ePD panel power enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_EN	S127	ePD panel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_PWM	S141	ePD panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
eDP0_HPD	S113	HPD Signal	I CMOS	1.8V	Runtime		
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.2.4 MIPI CSI1 (Camera)

MAS Elettronica SMARC modules have integrated a MIPI-CSI interface with up-to four data lanes and one clock lanes with MIPI D-PHY specification V1.2

The following table shows the pins of the SMARC connector are used when the MIPI CSI feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI1_RX0+ **CSI1_RX0-** **CSI1_RX1+** **CSI1_RX1-** **CSI1_RX2+** **CSI1_RX2-** **CSI1_RX3+** **CSI1_RX3-**	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY		Runtime		
CSI1_CK+ **CSI1_CK-**	P3 P4	CSI1 differential clock input (point to point)	I LVDS D-PHY		Runtime		
I2C_CAM1_DAT / ~~**CSI1_TX-**~~	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS MPHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_DAT MIPI-CSI 3.0 mode uses CSI1_TX-
I2C_CAM1_CK / ~~**CSI1_TX+**~~	S1	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_CK MIPI-CSI 3.0 mode uses CSI1_TX+
CAM1_PWR# / GPIO1	P109	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO1 can be enabled through DVT
CAM1_RST# / GPIO3	P111	Camera 0 reset, active low output	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO3 can be enabled through DVT
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		This signal is used by both CSI0 and CSI1

4.2.5 I2S (Audio)

MAS Elettronica SMARC module has integrated a I2S interface The I2S (or I2S) module provides a synchronous audio interface (SAI) that supports full-duplex serial interfaces with frame synchronization.

The following table shows the pins of the SMARC connector are used when the MIPI CSI feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2S0_LRCK	S39	I2S0 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S0_SDOUT	S40	I2S0 Digital audio Output	O CMOS	1.8V	Runtime		
I2S0_SDIN	S41	I2S0 Digital audio Input	I CMOS	1.8V	Runtime		
I2S0_CK	S42	I2S0 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S2_LRCK	S50	I2S2 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S2_SDOUT	S51	I2S2 Digital audio Output	O CMOS	1.8V	Runtime		
I2S2_SDIN	S52	I2S2 Digital audio Input	I CMOS	1.8V	Runtime		
I2S2_CK	S53	I2S2 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AUDIO_MCK	S38	Master clock output to I2S co-dec(s)	O CMOS	1.8V	Runtime		

4.2.6 USB 2.0 Ports

MAS Elettronica SMARC module has integrated a USB Hub 2.0.

The following table shows the pins of the SMARC connector are used when the USB HUB feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ **USB0-**	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Runtime		From SOC
USB0_EN_OC#	P62	USB over-current sense for port 0	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB0_VBUS_DET	P63	USB port 0 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Runtime		Can be connected to a USB client port VBUS pin
USB0_OTG_ID	P64	Input pin to announce OTG device insertion on USB 2.0 port	I CMOS	3.3Vsb / 3.3V	Runtime		
USB1+ **USB1-**	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Runtime		From USB HUB
USB1_EN_OC#	P67	USB over-current sense for port 1	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB2+ **USB2-**	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Runtime		From USB HUB
~~**USB2_SSRX+**~~ ~~**USB2_SSRX-**~~	~~S74~~ ~~S75~~	~~Receive signal differential pairs for SuperSpeed on port 2~~	~~I~~ ~~USB SS~~	~~USB SS~~	~~Runtime~~		

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
~~**USB2_SSTX+**~~ ~~**USB2_SSTX-**~~	~~S71~~ ~~S72~~	~~Transmit signal differential pairs for SuperSpeed on port 2~~	~~O USB SS~~	~~USB SS~~	~~Runtime~~		
USB2_EN_OC#	P71	USB over-current sense for port 2	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB3+ **USB3-**	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Runtime		From USB HUB
~~**USB3_SSRX+**~~ ~~**USB3_SSRX-**~~	~~S65~~ ~~S66~~	~~Receive signal differential pairs for SuperSpeed on port 3~~	~~I USB SS~~	~~USB SS~~	~~Runtime~~		
~~**USB3_SSTX+**~~ ~~**USB3_SSTX-**~~	~~S62~~ ~~S63~~	~~Transmit signal differential pairs for SuperSpeed on port 3~~	~~O USB SS~~	~~USB SS~~	~~Runtime~~		
USB3_EN_OC#	P74	USB over-current sense for port 3	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~**USB3_VBUS_DET**~~	~~S37~~	~~USB port 3 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Runtime~~		
~~**USB3_OTG_ID**~~	~~S104~~	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I CMOS~~	~~3.3Vsb / 3.3V~~	~~Runtime~~		
USB4+ **USB4-**	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Runtime		
USB4_EN_OC#	P76	USB over-current sense for port 4	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
~~**USB5+**~~ ~~**USB5-**~~	~~S59~~ ~~S60~~	~~USB differential data pairs for port 5~~	~~I/O~~ ~~USB~~	~~USB~~	~~Standby~~		
~~**USB5_EN_OC#**~~	~~S55~~	~~USB over-current sense for port 5~~	~~I/O OD CMOS~~	~~3.3Vsb / 3.3V~~	~~Standby~~	~~PU 10k~~	~~Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.~~

4.2.7 PCIe Port

MAS Elettronica SMARC module supports one PCIe Gen 2.1 ports (PCIE_A).

The following table shows the pins of the SMARC connector are used when the PCIe feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
PCIE_A_TX+ **PCIE_A_TX-**	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_A_RX+ **PCIE_A_RX-**	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_A_REFCK+ **PCIE_A_REFCK-**	P83 P84	Differential PCIe Link A reference clock output	O LVDS PCIE		Runtime		
PCIE_A_RST#	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		
PCIE_WAKE#	S146	PCIe wake up interrupt to host – com-mon to PCIe links A, B, C, D	I OD CMOS	3.3V	Runtime	PU 10k	

4.2.8 LAN Port

MAS Elettronica SMARC module supports one LAN port is derived from the SOCs RGMII interface

The following table shows the pins of the SMARC connector are used when the PCIe feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ **GBE0_MDI0-** **GBE0_MDI1+** **GBE0_MDI1-** **GBE0_MDI2+** **GBE0_MDI2-** **GBE0_MDI3+** **GBE0_MDI3-**	P30 P29 P27 P26 P24 P23 P20 P19	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	GBE MDI		Runtime		Twisted pair signals for external transformer.
GBE0_LINK100#	P21	Link Speed Indication LED for GBE 0 100Mbps	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE0_LINK1000#	P22	Link Speed Indication LED for GBE 0 1000Mbps	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
							LED current
~~**GBE0_CTREF**~~	~~P28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~	~~Analog~~	~~0 to 3.3V max~~	~~Runtime~~		
GBE0_SDP	P6	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)	IO CMOS	3.3V	Runtime		

4.2.9 SDIO Port

MAS Elettronica SMARC module supports one one MMC/SD/SDIO port. The port is derived from the i.MX8M Mini on-chip MMC/SD/SDIO controller (uSDHC2)

The following table shows the pins of the SMARC connector are used when the SDIO feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_D0 **SDIO_D1** **SDIO_D2** **SDIO_D3**	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to en-able the power being supplied to a SD/MMC card device.	O CMOS	3.3V	Runtime		should be driven low in STB Mode by the module

4.2.10 SPI0 Port

MAS Elettronica SMARC module supports one SPI port. Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes.

The following table shows the pins of the SMARC connector are used when the SPI0 feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
SPI0_CS1#	P31	SPI0 Master Chip Select 1	O CMOS	1.8V	Standby		
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Standby		
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

4.2.11 QSPI (ECSPI) Port

MAS Elettronica SMARC module supports one Quad SPI serial flash devices, each with up to four bidirectional data lines.

loopback mode)The following table shows the pins of the SMARC connector are used when the QSPI feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ESPI_CS0#	P54	ESPI1 Master Chip Select 0	O CMOS	1.8V	Standby		
ESPI_CS1#	P55	ESPI1 Master Chip Select 1	O CMOS	1.8V	Standby		
ESPI_CK	P56	ESPI Master Clock output	O CMOS	1.8V	Standby		
ESPI_RESET#	S58	ESPI Reset	O CMOS	1.8V	Standby		Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves
ESPI_ALERT0# **ESPI_ALERT1#**	S43 S44	ESPI ALERT	I OD CMOS	1.8V	Standby		This pin is used by eSPI slave to request service from eSPI.master. Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.
ESPI_IO_0 **ESPI_IO_1** **ESPI_IO_2** **ESPI_IO_3**	P58 P57 S56 S57	ESPI Master Data Input / Out-put.	I/O CMOS	1.8V	Standby		ESPI_IO_0 can also be used as SPI1_DO (MOSI) ESPI_IO_1 can also be used as SPI1_DIN (MISO) In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO).

4.2.12 General purpose I2C

The SMARC specification supports a total of 6 different I2C busses on its pinout. Most of these busses are designated for specific functions such as I2C for camera management, LVDS panels or I2C for PMIC. Just one I2C bus is marked as General purpose.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2C_GP_DAT	S49	General purpose I2C data signal	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_GP_CK	S48	General purpose I2C clock signal	O OD CMOS	1.8V	Runtime	PU 2k2	

Most of the other I2C busses are described in their designated function tables rather than in a single big list.

Below is an overview of all I2C busses and where to find them.

Name	Pin #	Description	Where to find
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	LVDS / DSI / eDP tables
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	LVDS / DSI / eDP tables
I2C_CAM1_DAT	S2	I2C data for serial camera data support link	MIPI CSI table
I2C_CAM1_CK	S1	I2C clock for serial camera data support link	MIPI CSI table
I2C_PM_DAT	P122	Power management I2C bus DATA (SMBus for x86)	Power and System Management
I2C_PM_CK	P121	Power management I2C bus CLK (SMBus for x86)	Power and System Management

4.2.13 General purpose I/O (GPIO)

MAS Elettronica SMARC modules supports one 12 GPIO lines that are required by the SMARC 2.11 standard.

The following table shows the pins of the SMARC connector are used when the GPIO feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470K on the Mod-ule.	Default use is GPIO0
GPIO1	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is is GPIO1
GPIO2	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO2
GPIO3	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO3
GPIO4	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO5	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO6	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO7	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO8	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO9	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO10	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO11	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	

4.2.14 UART

Anita i.MX8M Mini the module supports 4 universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP.
The following table shows the pins of the SMARC connector are used when the UART feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER0_TX	P129	Asynchronous serial data output port 0	O CMOS	1.8V	Runtime		
SER0_RX	P130	Asynchronous serial data input port 0	I CMOS	1.8V	Runtime		
SER0_RTS#	P131	"Request to Send" handshake line for port 0	O CMOS	1.8V	Runtime		
SER0_CTS#	P132	"Clear to Send" handshake line for port 0	I CMOS	1.8V	Runtime		
SER1_TX	P134	Asynchronous serial data output port 1	O CMOS	1.8V	Runtime		
SER1_RX	P135	Asynchronous serial data input port 1	I CMOS	1.8V	Runtime		
SER2_TX	P136	Asynchronous serial data output port 2	O CMOS	1.8V	Runtime		
SER2_RX	P137	Asynchronous serial data input port 2	I CMOS	1.8V	Runtime		

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER2_RTS#	P138	"Request to Send" handshake line for port 2	O CMOS	1.8V	Runtime		
SER2_CTS#	P139	"Clear to Send" handshake line for port 2	I CMOS	1.8V	Runtime		
SER3_TX	P140	Asynchronous serial data output port 3	O CMOS	1.8V	Runtime		
SER3_RX	P141	Asynchronous serial data input port 3	I CMOS	1.8V	Runtime		

4.2.14 CAN BUS

Anita i.MX8M Mini the module supports 2 CAN V2.0B at 1 Mb/s using the MCP2515 SPI CAN controller.
The following table shows the pins of the SMARC connector are used when the CAN feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	3.3V	Runtime		
CAN0_RX	P144	CAN port 0 Receive input	I CMOS	3.3V	Runtime		
CAN1_TX	P145	CAN port 1 Transmit output	O CMOS	3.3V	Runtime		
CAN1_RX	P146	CAN port1 Receive input	I CMOS	3.3V	Runtime		

4.2.15 Miscellaneous

The following table shows the pins of the SMARC connector are used when the Miscellaneous feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Do-main	PU / PD	Comments
TEST#	S157	Held low by Carrier to invoke Module vendor specific test function(s).	I CMOS	1.8V	Runtime	PU on Mod-ule. Driven by OD on Carrier	Module must implement PU but actual value is depended on particular module design. Carrier Board should leave this pin floating for normal operation

4.2.16 Power and System Management

The following table shows the pins of the SMARC connector are used when the Power and System Management feature is enabled.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CARRIER_PWR_ON	S154	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8Vsb / 1.8V	-		1.8Vsb is only used for signaling, not a power source to the module
CARRIER_STBY#	S153	The Module shall drive this signal low when the system is in a standby power state.	O CMOS	1.8Vsb / 1.8V	-		
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
VIN_PWR_BAD#	S150	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.	I OD CMOS	1.8V	Runtime	PU 2.2K	Driven by OD on Carrier Module must implement PU but actual value is depended on particular module design.
SLEEP#	S149	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state.Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
POWER_BTN#	P128	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	1.8V	Runtime		
RESET_IN#	P127	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	1.8V	Runtime	PU 4.7K	Driven by OD on Carrier. Pulled up on module.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB DATA. Pulled up on module.
I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB CLK. Pulled up on module.
SMB_ALERT_1V8#	P1	SMBus Alert# (interrupt) signal	I OD CMOS	1.8V	Runtime	PU 2k2	only used on x86 design

4.2.17 Boot Select

The following table shows the pins of the SMARC connector are used when the Boot selection.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# **BOOT_SEL1#** **BOOT_SEL2#**	P123 P124 P125	Input straps determine the Module boot	I OD CMOS	1.8Vsb	Standby	PU 4.7K	Driven by OD on Carrier. Pulled up on module. Booting from EMMc and SDcard is supported
FORCE_RECOV#	S155		I OD CMOS	1.8Vsb	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module.

4.2.18 Power

The following table shows the pins of the SMARC connector are used for the power supply of the board.

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max	P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?	3 to 5.25V / 5V		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?	Ground		

4.2.19 HDMI

In the MIN Board the HDMI can be drived from:

1) SMARC Connector

2) Lontium LT8912B

The following table shows the pins of the SMARC connector are used for the power supply of the board.

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
HDMI_D2+ **HDMI_D2-** **HDMI_D1+** **HDMI_D1-** **HDMI_D0+** **HDMI_D0-**	P92 P93 P95 P96 P98 P99	HDMI port, differential pair data lines	O TMDS HDMI	Runtime		
HDMI_CK+ **HDMI_CK-**	P101 P102	CK HDMI port, differential pair clock lines O	O TMDS HDMI	Runtime		
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDM	O OD COMS	1,8V	4,7K	
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	I/O OD COMS	1,8V	4,7K	

4.2.20 WiFi Client/AP module

In the MINA Board is present a WiFi Module from uBLOX LILY-W133-10B with integrated antenna.

Below some of the Main Features:

Feature	Commets
Chip inside **Wi-Fi output power EIRP [dBm]** **Wi-Fi micro access point [max stations]** **Wi-Fi standards (IEEE 802.11)**	NXP 88W8801 15 8 IEEE 802.11b, IEEE 802.11g, IEEE 802.11n
AES hardware support **Factory calibrated RF** **Factory programmed MAC address(es)** **MAC address stored in module** **Wi-Fi direct** **WPA3**	YES YES YES YES YES YES

For more info about the module :

LILY-W1 series | u-blox

5.0 Module Outline – 82mm x 50mm SMARC Module

The Figure 2 on the following page details the 82mm x 50mm ANITA-iMX8M Mini mechanical attributes, including the pin numbering and edge finger pattern.

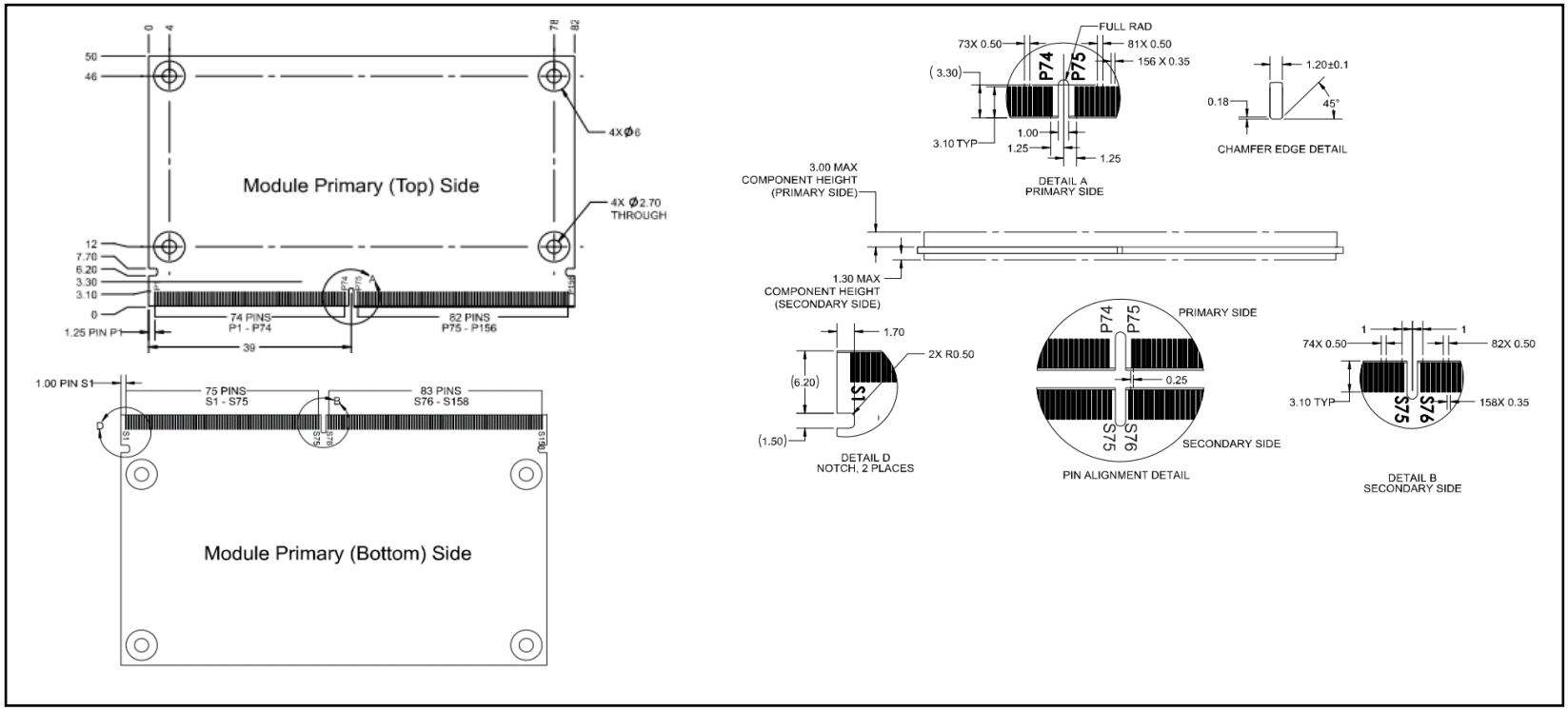
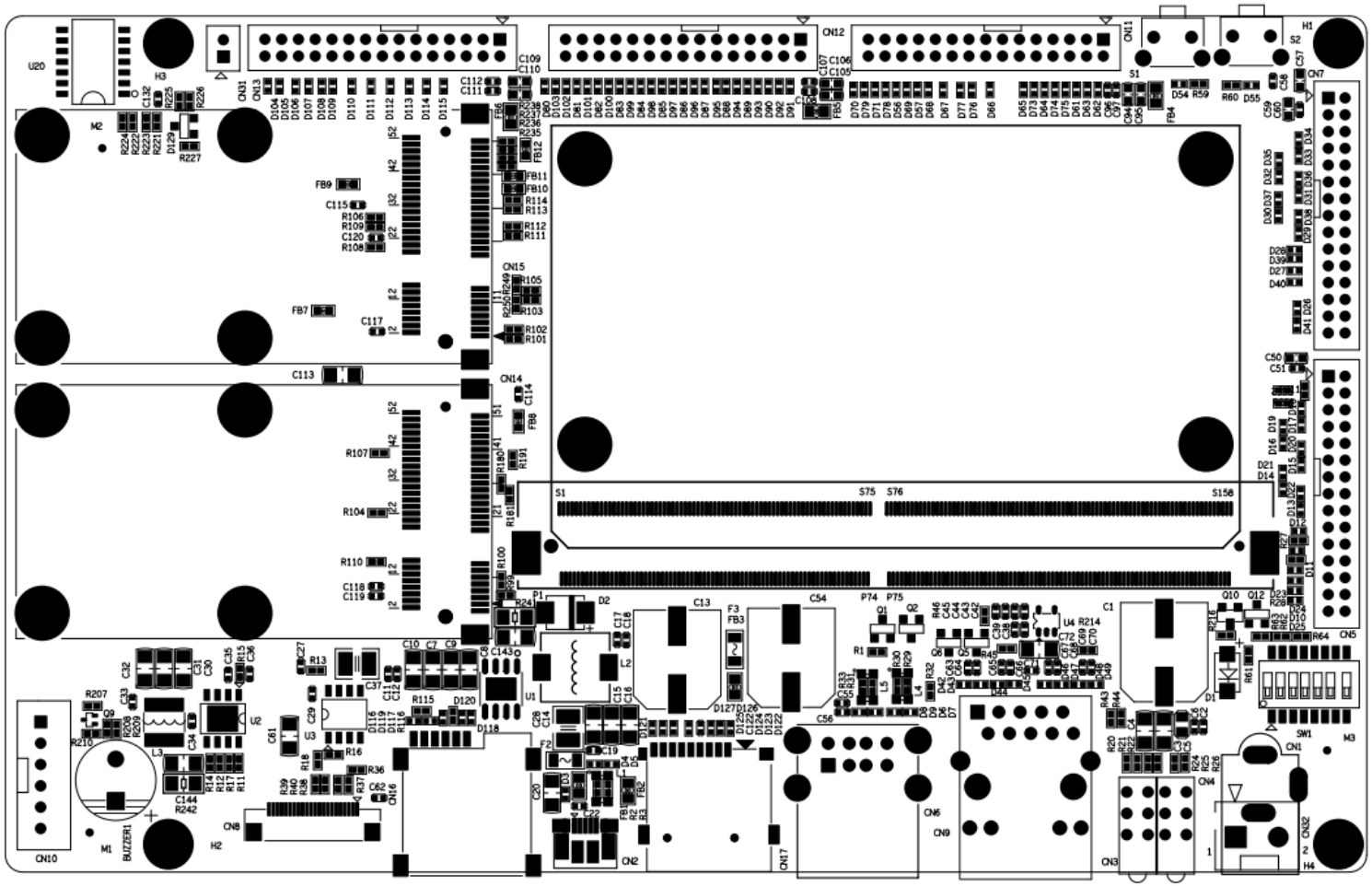


Figure 4 Module Outline

7.0 Carrier Outline – 102mm x 146mm



Technical Support and Warranty

Technical Support

MAS Elettronica provides its product with one-year free technical support including:

1. Providing software and hardware resources related to the embedded products of MAS Elettronica;
2. Helping customers properly compile and run the source code provided by MAS Elettronica;
3. Providing technical support service if the embedded hardware products do not function properly under the circumstance that customers operate according to the instructions in the documents provided by MAS Elettronica;
4. Helping customers troubleshoot the products.

T he following conditions will not be covered by our technical support service. We will take appropriate measures accordingly:

a. Customers encounter issues related to software or hardware during their development process;
b. Customers encounter issues caused by any unauthorized alter to the embedded operating system;
c. Customers encounter issues related to their own applications;
d. Customers encounter issues caused by any unauthorized alter to the source code provided by MAS Elettronica;

Warranty Conditions

12-month free warranty on the PCB under normal conditions of use since the sales of the product;
The following conditions are not covered by free services; MAS Elettronica will charge accordingly:

Customers fail to provide valid purchase vouchers or the product identification tag is damaged, unreadable, altered or inconsistent with the products.
Products are damaged caused by operations inconsistent with the user manual;
Products are damaged in appearance or function caused by natural disasters (flood, fire, earthquake, lightning strike or typhoon) or natural aging of components or other force majeure;
Products are damaged in appearance or function caused by power failure, external forces, water, animals or foreign materials;
Products malfunction caused by disassembly or alter of components by customers or, products disassembled or repaired by persons or organizations unauthorized by MAS Elettronica, or altered in factory specifications, or configured or expanded with the components that are not provided or recognized by MAS Elettronica and the resulted damage in appearance or function;
Product failures caused by the software or system installed by customers or inappropriate settings of software or computer viruses;
Products purchased from unauthorized sales;
Warranty (including verbal and written) that is not made by MAS Elettronica and not included in the scope of our warranty should be fulfilled by the party who committed. MAS Elettronica has no any responsibility;

3 Within the period of warranty, the freight for sending products from customers to MAS Elettronica should be paid by customers; the freight from MAS Elettronica to customers should be paid by us. The freight in any direction occurs after warranty period should be paid by customers.
4 Please contact technical support if there is any repair request.

Note:

MAS Elettronica will not take any responsibility on the products sent back without the permission of the company.

Contact Information

Phone: +39-0498687469

Sales: sm@maselettronica.com

Support: support@maselettronica.com

Website: http://www.maselettronica.com

Address: Via Rossi 1 35030 Rubano (PD) Italy