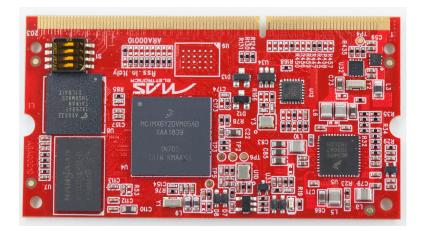
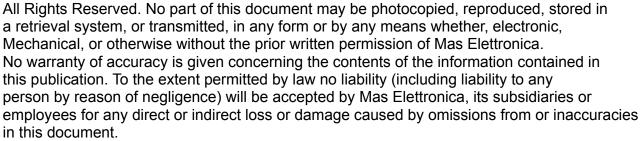


Aura iMX6UL/ iMX6ULL/ iMX6ULZ Module Rev 1.0





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Revision History..

Rev.	Document Code	Released	Written	Verified	Approved
1.0	Aura iMX6UL	16/10/2019	S.Mascetti	16/10/2019	S.Mascetti

Introduction

The AURA CPU is IMX6UL, IMX6ULL and IMX6ULZgeneral purpose system on module designed to work in Industrial, Automotive and consumer environment. The AURA CPU is Sodimm module with a small foot print ready be applied on the Application Board (Carrier Board).

Reference Documentation

- 1) IPC-A-610E Acceptability of Electronics Assemblies Training and Certification Program
- 2) IPC-A-600 Acceptability of Printed Boards Training and Certification Program
- 3) IPC-A-6011: Generic Performance Specification for Printed Boards
- 4) IPC-A-6012D: Qualification and Performance Specification for Rigid Printed Boards
- 5) RoHS II Directive 2011/65/EU and 2015/863/EU (2002/95/EC and successive amendments)
- 6) REACH Regulation (EC) No. 1907/2006
- 7) NXP iMX6UL Datasheet and Application Notes
- 8) NXP PF3000 DataSheet and Application Notes

Specification

Mechanical

AURA CPU PCB Board Dimensions

: 67,6X36,58 mm

Electrical

AURA CPU Processor Board : (+5Vdc +/- 5%) or +4Vdc (LiIon Cell)

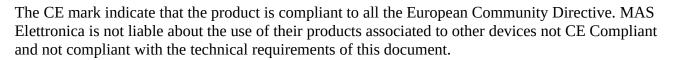
Temperature

The working temperature is -40°C to +85°C. The storage temperature is -40°C to +85°C.

Certifications

European CE Mark

The AURA CPU product is CE compliant



RoHS and REACH Directive

This product (include all the components, materials for packaging, etc.) must be compliant with the RoHS European directive 2002/95/CE (known as RoHS, Restriction on the use of certain Hazardous Substances) for the use of particular dangerous material on electrical equipment (AEE)

RoHS Directive 2011/65/EU EN 50581:2012 EN 62321:2009 **REACH Regulation (EC) No 1907/2006**

AURA CPU

The AURA CPU is the system on module based on NXP iMX6UL family that integrate the following peripherals / functions:

- NXP i.MX6UL, i.MX6ULL, i.MX6ULZ Application Processor
- 256MiB,512MiB or 1GiB of DDR3L Memory
- 4/8/16GB of eMMC Flash
- Real Time Clock
- LCD Interface (24Bit) (Optionally con be configured as General Purpose TTL 3V3 I/O)
- 3 Analog Input
- General Purpose I/O
- 6 UART Serial Port TTL 3V3 (RX TX)
- 2 CAN Port TTL 3V3 with Driver Enable I/O
- 2 I2C Bus TTL 3V3
- 2 SPI Bus TTL 3V3
- SDIO Bus TTL 3V3
- I2S Bus
- 1 USB OTG Port
- 1 USB 2.0 Port
- 1 10/100 Ethernet Port with physical on board
- 1 10/100 Ethernet MAC Port
- 5V Dc +/- 5%

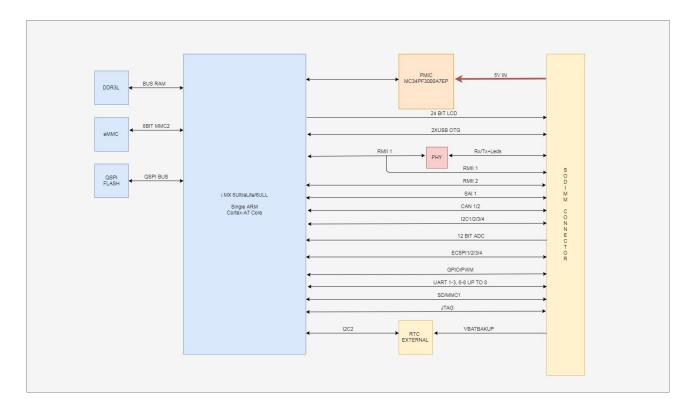
AURA CPU Operating System

LINUX Kernel Version 4.1.15 or later build with YOCTO

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Block Diagram



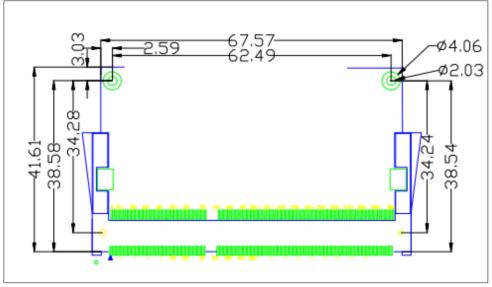
AURA CPU block diagram

Functionalities

Function	Туре	Description			
MEMORY	DDR3L Memory	The module is designed in order to support the following memory size/configuration: 256 MiB 1*256MB DDR3L 512MiB 1*512MB DDR3L 1GiB 1*1GiB DDR3L			
	eMMC Flash	The main FLASH memory of the module is an eMMC. The minimum size is 4/8/16GB. <i>On the eMMC are installed the Linux OS and uBoot.</i>			
	UART1 (Console)	This UART is used to communicate with the Linux Console TTL 3V3			
	UART23-4-6	This UARTs are available as RX and TX TTL 3v3 UART. The RS232 driver should be added on the Application Board. These UARTs could be used as RS485 or RS422 adding the transceiver into the Application Board and using the GPIO to drive the data direction			
	UART5	This UART is available RX, TX, CTS and RTS TTL 3V3. The UART5 could be used to connect devices that are using RTS and CTS (example BT Modules).			
COMs	Ethernet	The iMX6UL processor integrate 2 Ethernet Controller ETH0 and ETH1. The Physical Driver for ETH0 are present on the AURA CPU, and on the Castellated Connectors there are available the Signals to connect the Magnetic and RJ45. Link and activity LED signals are present in the Castellated Connector The MAC signal of ETH1 are available on the Castellated Connector. The Physical Driver have to be			
		 added on the Application Board in case the second ETH is required. <i>The MDx pins of ETH1 pins can be configured as GPIO.</i> <i>The MC Bus to configure the Physicals is shared between ETH0 and ETH1 MAC Controllers</i> 2 CAN Port are provided by the iMX6UL processor. The CAN RX / TX are TTL 3V3 and the CAN 			
	CAN Port	Driver is not present on the board.			
	SDIO	The SDIO Bus function is provided by the iMX6UL Processor. This Bus can be used to connect a Flash Memory Card or other devices that are using this kind of communication Bus (example combo WIFI and BT Module). The SDIO Bus could be 3V3 or TTL 1.8V Voltage level selectable on PMU PF3000.			
Expansin BUS	12S	The I2S bus function is provided by the iMX6UL Processor. The signals are TTL 3V3 level and can be software configured as GPIO			
	SPI	2 SPI bus, SPI0 and SPI1, are available on the Castellated Connector. The Bus are TTL 3V3			
	I2C	1 12C bus is available on the Castellated Connector The Bus are TTL 3V3 The internal PMU PF3000 is connected on this 12C2 Bus.			
Digital &	LCD/GPIO	An 24Bit LCD controller is present on the iMX6UL5 Processor. If the LCD Function is not used the pins can be software configured as GPIO. The voltage level is configurable from 1.8V and 3.3V on PMU PF3000			
AnalogI I/O	ANALOG	3 Analog Input are present on the iMX6UL Processor. The voltage Input level is 3.3VMax These pins can be software configured as GPIO			
LICD	USB1	This port is an USB2.0 OTG Device/Host Mode.			
USB	USB0	This port is an USB2.0 Host Only Mode and does not have a 5V power over current protection			
	RTC	The Real Time Clock function is integrated on the iMX6UL Processor. Battery Back-up have to be provided on the Application Board			
	PMU	The Power Management is performed by the PF3000.			

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Aura Module Dimentions



Dimentions of Aura Module

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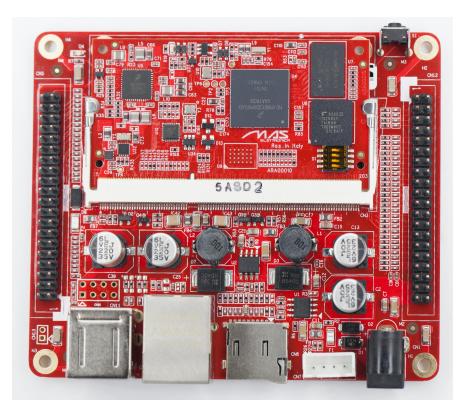


Carrier Board Sara for Aura i.MX6ULL

Aura has a dedicated carrier board SARA.

With the following characteristics:

- SD/ MMC x1
- 2 USB Host, 1x USB OTG
- UART x2
- I2C x2
- SPI x2
- RTC x1
- Ethernet x1
- GPIOs x30
- Display LCD TTL
- Touch screen interface resistive of capacitive
- Power supply 12VDC
- Dimetions 130 x 103.5 mm



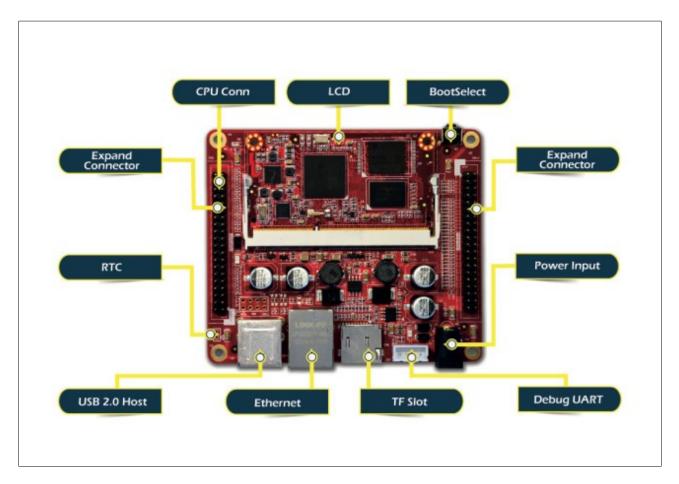
SARA with Aura CPU

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Rev 1.0





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Sara Block Diagram and Connectors



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